SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_{1-X}Ga_XSe_2$- BASED SOLAR CELLS***

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PART I – CdTe

1.0 INTRODUCTION

This annual report covers activities performed during the second year of this project. Work related to further advancing performance and understanding performance limitations is primarily focused on "thin CdS" coupled with the use of "buffers" (resistive) oxide layers. In this report results for Zn-Sn-O films and devices based on these are presented; In_2O_3 has also been used as a buffer layer. A dry back contact process has also been investigated, where the typical wet processing (i.e. Br_2 or NP etch) has been eliminated. The use of Cu and its role in CdTe cells has also been further investigated. A new approach to introducing Cu in CdTe cells is presented with interesting results on the effect of this element on device performance. Experimental details will be provided within the appropriate sections that follow. Cell analysis is based on basic solar cell measurements such as dark and light current-voltage (J-V), monochromatic J-V, spectral response (SR), and capacitance-voltage (C-V) measurements. Whenever appropriate, additional analysis is carried out in collaboration with NREL or other CdTe Thin Film Partnership members.

2.0 SUMMARY OF FABRICATION PROCEDURES

Table 1 summarizes the various processes and materials utilized for this project. Additional details will be provided within the sections that follow.

Table 1. Summary of processes and materials utilized for the fabrication of CdTe solar cells.

	Materials	COMMENTS
Substr.	7059 Borosilicate Glass; Soda lime glass (TEC 15)	Cleaned in dilute HF solution (1:10)
Transparent Contact	SnO_2:F	by MOCVD (Tetramethyltin, O_2, F-source: Halocarbon 13B1)
	Cd_2SnO_4	by co-sputtering of CdO and SnO_2
	$CdIn_2O_4$	by reactive co-sputtering of Cd and In
	ITO	by sputtering of In_2O_3:Sn
Buffer Layer (high-ρ)	SnO_2	by MOCVD (as above; undoped)
	SnO_2	by sputtering of Sn (reactive) or SnO_2 targets
	Zn_2SnO_4	by co-sputtering of ZnO and SnO_2
	$ZnIn_2O_4$	by reactive co-sputtering of Zn and In
	In_2O_3	by reactive sputtering of In
CdS		by: (a) CBD and (b) CSS
CdTe		by CSS: (a) small area reactor for baseline devices; (b) large area (10 x 10 cm^2) deposition with substrate motion
$CdCl_2$ HT		(a) Direct application of $CdCl_2$ by evaporation followed by HT; (b) Exposure of CdTe surface to $CdCl_2$ vapors
Back Contact	Graphite	(a) doped with HgTe:Cu (baseline); (b) undoped (used as received)
	Mo	by sputtering
	Sb_2Te_3/Mo	by sputtering
	Cu_XTe/Mo	by sputtering
	Cu/back electrode	Cu deposited by sputtering; back electrode: undoped graphite or Mo

3.0 ALTERNATIVE WINDOW LAYERS – TRANSPARENT OXIDES/BUFFERS

Most work in this area is focused on transparent oxides to be used as "buffer" (or high-ρ) layers. As already indicated in table 1, the transparent "buffers" are based on binary and ternary compounds of Sn, Zn, and In. Additional information on the deposition processes (primarily sputtering) has been included in a previous report [1]. The use of a bi-layer front contact (i.e. low-ρ/high-ρ) is beneficial to device performance for both CdTe and CIGS devices. In CdTe cells the ultimate objective would be to eventually replace CdS, and therefore gain approximately 7 mA/cm^2 in J_{SC}, or simply use a very thin layer of CdS that will transmit most of the energy that lies above its bandgap (<510 nm).

Information on material properties (for Cd_2SnO_4, SnO_2, In_2O_3 and $CdIn_2O_4$) and their dependence on deposition conditions has been included in last year's report and other publications [2,3]. In this report we include xrd data for Zn-Sn-O (ZTO) films. Zinc stannate (Zn_2SnO_4) has been used by the CdTe group at NREL for the fabrication of the highest efficiency CdTe cells to-date [4]. Although a Zn/Sn ratio of 2.0 (i.e. Zn_2SnO_4) has been emphasized for this work, Zn-Sn-O films of other compositions (1.0 < Zn/Sn < 2.5) are also being considered. The composition of the as-deposited films is varied by adjusting the individual deposition rates of ZnO and SnO_2. The term Zn/Sn ratio as used in this report refers to the as-deposited film composition. The Zn/Sn ratio has been calibrated using EDS measurements to determine the composition of the as-deposited films. Early results indicated that as-deposited Zn-Sn-O films are mostly amorphous, and similar to the Cd_2SnO_4 films must be heat-treated in order to crystallize. In addition to Zn_2SnO_4, In_2O_3 was also used as a buffer layer and device results are presented in this report that demonstrate the potential of this material as an effective front contact component for CdTe cells. Resistivity and XRD data for In_2O_3 have been reported in the Phase I report.

3.1 Zn-Sn-O Films

3.1.1 Crystallographic Properties – The Effect of Annealing

As indicated above, initial work with this material focused on depositing films with a Zn/Sn ratio of 2.0, although recently films with Zn/Sn ratio of 1.0 to 2.5 have also been preapred. Figure 1 shows XRD data for several ZTO films (Zn/Sn=2.0) deposited at room temperature on SnO_2:F coated glass substrates, and subsequently annealed in He ambient (partial vacuum). Although, plain glass substrates are also used as substrates, most of the present work has been on ZTO films deposited on SnO_2:F/glass substrates, in order to study the actual structures that will eventually be utilized for solar cell fabrication. Figure 1includes the XRD pattern of a SnO_2:F film as a reference (top); 2θ values of 26.15, 52.01, 54.47, and 66.19º are all associated with SnO_2. The XRD pattern for the as-deposited ZTO film is essentially identical to that obtained for the SnO_2:F substrate, suggesting that ZTO deposited at room temperature is amorphous; it is possible that the SnO_2 phase may be present in ZTO, but due to the substrate this cannot be seen; however, this is not believed to be the case, as preliminary data on glass substrates for similar ZTO films show no signs of any SnO_2 formation. Annealing at 550 ºC shows little change (if any) in the XRD pattern of ZTO. The two films annealed at 575 and 600 ºC, clearly show additional peaks, associated with the Zn_2SnO_4 phase; the highest intensity Zn_2SnO_4 peak is marked with a dotted vertical line in Fig. 1 and corresponds to the [311] direction. An expanded view of the same data is shown in Fig. 2 marking several Zn_2SnO_4 peaks. No additional phases have been definitively identified to this point, with the exception of $ZnSnO_3$ which may be present in some films. Annealing temperatures higher than those indicated in Figs. 1 and 2 have also been utilized during preliminary studies, but based on solar cell performance data the optimum range has been identified to be 575-600 ºC, which is the reason

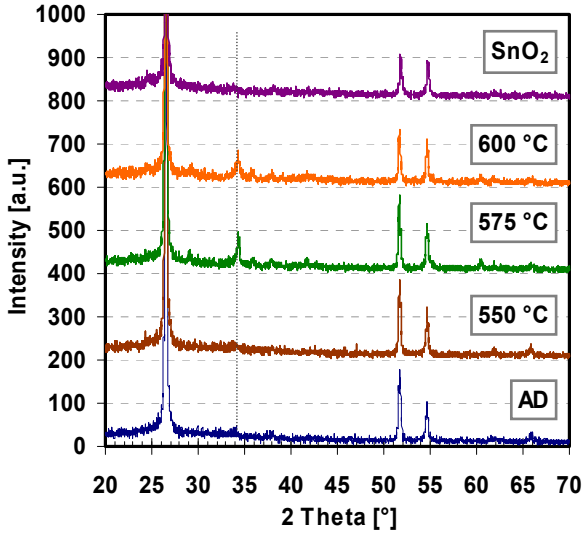

Figure 1. XRD data for Zn-Sn-O films deposited on SnO_2 and heat-treated at various temperatures

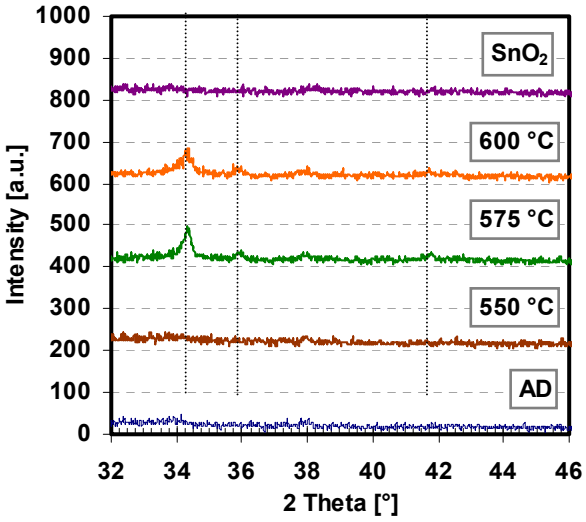

Figure 2. The 2θ range from 32 to 46º identifying Zn_2SnO_4 peaks; (311) (222) and (400)

that presently annealing temperatures are limited to 600 ºC. Preliminary results for ratios other than Zn/Sn=2.0 indicate that for for Zn/Sn near or above 2.0 the Zn_2SnO_4 is prevalent, while at ratios less than 2.0 (1.5) the $ZnSnO_3$ (orthorhombic) phase is present.

3.1.2 Optical Transmission

The optical transmission of Zn-Sn-O films is being measured in the range of 400-900 nm. Figures 3 and 4 show transmission data for Zn-Sn-O films prepared under various conditions and subsequently annealed (in He ambient). Figure 3 compares the optical transmission of films deposited with a Zn/Sn ratio of 2.0 (similar to films described in Fig. 1). Figure 4 shows the optical transmission of Zn-Sn-O films deposited at various Zn/Sn ratios and annealed at 600 ºC.

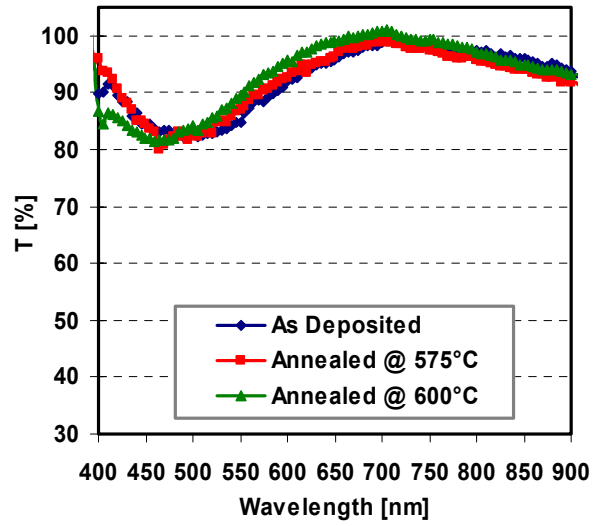

Figure 3. Optical transmission of Zn-Sn-O films deposited with a Zn/Sn ration of 2.0 and annealed in He ambient

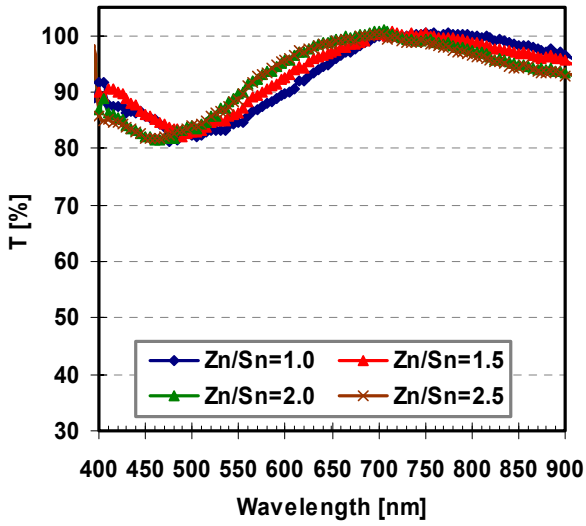

Figure 4. Optical transmission of Zn-Sn-O films deposited at various Zn/Sn ratios and annealed at 600 ºC

In all cases the optical transmission is on average just above 90%, and does not seem to be affected either by film composition or crystallinity.

3.1.3 Solar Cell Results - Zn/Sn=2.5

This section includes device results for CdTe/CdS solar cells fabricated on Zn-Sn-O/SnO_2:F/glass substrates. The main objective is to optimize the performance of Zn-Sn-O based solar cells, and understand the influence of this buffer on the overall device characteristics and processing. The CdS and CdTe films are deposited using baseline processes; CBD for CdS and CSS for CdTe; all CdS films had the same starting thickness of approx. 800-900 Å. The back contact is HgTe;Cu doped graphite. The $CdCl_2$ treatment is carried out by first evaporating $CdCl_2$ on CdTe, and subsequently heat treating the structures (in He/O_2 ambient); the temperature of this process has been typically varied in the range of 380-420 ºC.

3.1.3.1 Zn/Sn=2.5 – Effect of Heat Treatment

Figure 5 shows the J-V and SR characteristics for four devices fabricated on ZTO/SnO_2:F/glass substrates (legend values indicate the ZTO annealing temperatures). In this case the ZTO films were deposited with a Zn/Sn ratio of 2.5. The only processing variation is the ZTO annealing temperature (prior to the deposition of CdS); they were used (a) as-deposited (amorphous), and (b) heat-treated at 550, 575, and 600°C in inert ambient; the $CdCl_2$ heat treatment was carried out at 400°C. It is clear that the dark J-V "degrade" (i.e. dark currents increase) as the annealing temperature of ZTO decreases, with the device fabricated on as-deposited (AD) ZTO exhibiting the highest dark current. The QE data suggests that the CdS for the AD-ZTO device has been entirely "consumed" during the fabrication process, while for the cells fabricated on heat treated ZTO it appears that the CdS thickness (i.e. blue QE) is the same. However, the red response for the 600°C device is improved indicating improvement in collection for that device. Based on these results it appears that junction quality improved (i.e. dark currents decrease) with increasing annealing temperature. The SR data also suggest that amorphous ZTO films lead to "excessive" CdS consumption; although consumption of CdS can be viewed as being beneficial due to the improved blue SR, it comes at the expense of higher dark currents which cause a decrease in V_{OC} and FF. Figure 6 shows the V_{OC} and FF for the devices discussed in this section. Clearly, increasing the annealing temperature results in improved

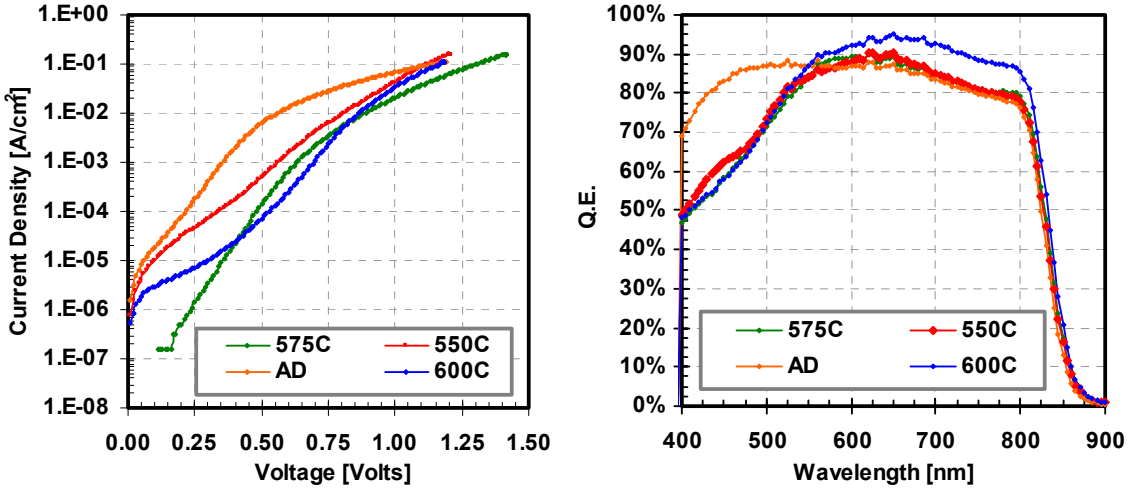

Figure 5. Dark J-V and SR characteristics for CdTe/CdS solar cells fabricated on ZTO(Zn/Sn=2.5)/SnO_2:F/glass substrates; (T_{CdCl2}=400ºC)

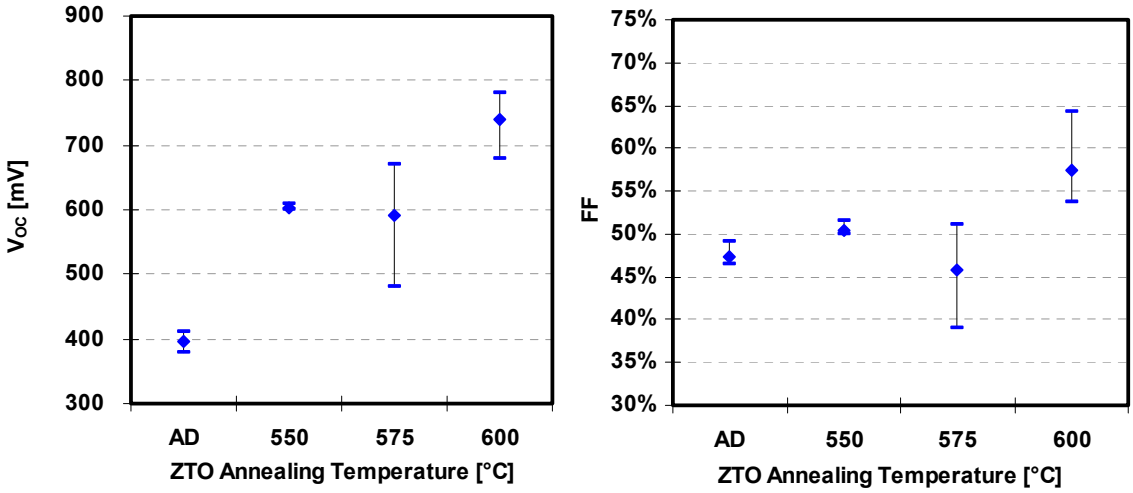

Figure 6. The V_{OC} and FF for CdTe cells of Fig. 5 shown as a function of the ZTO annealing temperature; (T_{CdCl2}=400ºC)

performance. Higher annealing temperatures did not result in further improvements; in certain cases higher annealing temperatures also resulted in peeling or cracking of the ZTO films.

Figure 7 displays the dark J-V and SR for cells fabricated using the same type of substrates as the devices shown in Fig. 5; the only difference is that the devices shown in Fig. 7 have been $CdCl_2$-heat-treated at 420 °C (vs. 400 °C for the cells in Fig. 5). The overall trends shown in the two figures are similar; in both cases the dark currents increase with decreasing annealing temperature of the ZTO with the AD-ZTO devices exhibiting the highest dark currents. The higher $CdCl_2$ annealing temperature seems to lead to higher dark currents for the 550 and 575 °C heat treated ZTO devices, with no apparent differences observed for the 600 °C device. The same is true for the SR of these cells; the red response (collection) of the AD, and annealed at 550 and 575 °C, appears improved (compared to the devices annealed at 400°C). A summary of the performance characteristics for the cells shown in Fig. 7 is provided in Fig. 8. Overall device performance improves with increasing annealing temperature; comparing the results shown in Figs 6 and 8, there appears to be no clear choice with regards to the $CdCl_2$ annealing

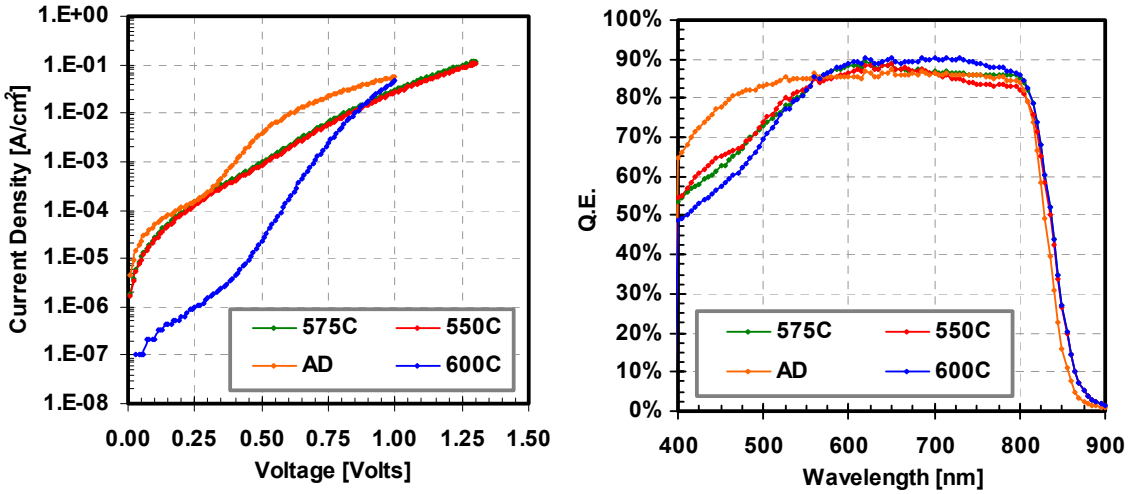

Figure 7. Dark J-V and SR characteristics for CdTe/CdS solar cells fabricated on ZTO(Zn/Sn=2.5)/SnO_2:F/glass substrates; (T_{CdCl2}=420ºC)

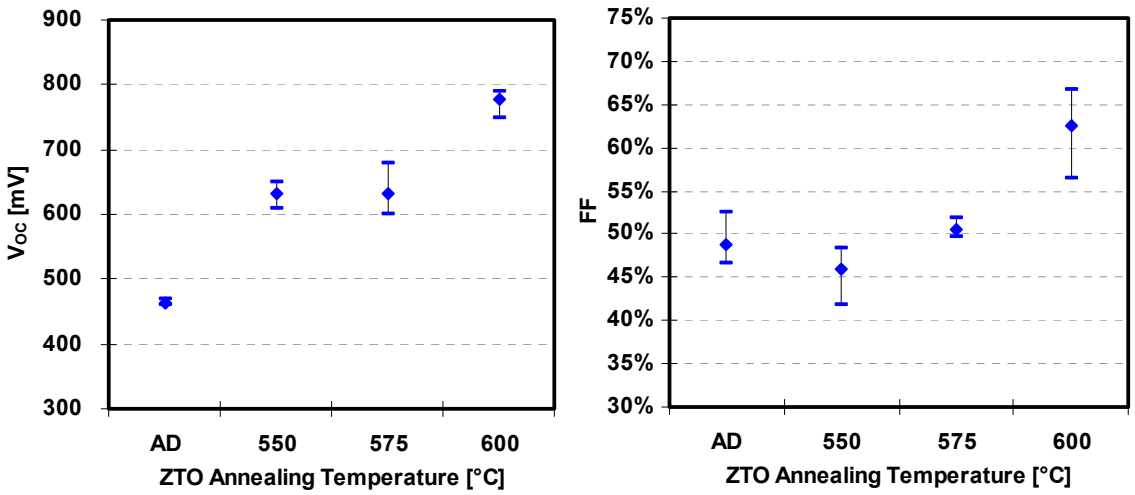

Figure 8. The V_{OC} and FF for CdTe cells of Fig. 7 shown as a function of the ZTO annealing temperature; (T_{CdCl2}=420ºC)

temperature since to first order there are no significant differences in performance. This is not typical behavior; for other front contact materials (for example SnO_2 bi-layers), the increase in $CdCl_2$ annealing temperature results in significant drop in performance (all other parameters being the same). Therefore the results obtained with Zn-Sn-O suggest that this material increases the processing "window" for the $CdCl_2$ heat treatment process.

3.2 In_2O_3

Resistivity and XRD data on In_2O_3 films have been presented in last year's report [1]. The resitsivity of In_2O_3 was found to be in the range of 1-10 Ω-cm, depending on the deposition temperature. In this report solar cells fabricated with this material as a buffer or high-ρ layer are presented. The TCO was In_2O_3:Sn (ITO). Both were deposited by sputtering (see table 1). For cells discussed in this section both ITO and In_2O_3 were deposited at 300 ºC substrate temperature.

3.2.1 ITO/ In_2O_3 - based Solar Cells

The light J-V characteristics for CdTe cells fabricated on ITO/In_2O_3 bi-layers, at various In_2O_3 thicknesses are shown in Fig. 9. The J-V behavior around V_{OC}, of the cell fabricated directly on on ITO (without the high-ρ In_2O_3), suggests that the ITO/CdS interface presents a barrier (i.e. rectifying front contact) in these devices; at this time this is believed to be due to the surface properties of ITO; it has been reported that depending on the O_2 concentration on the surface of ITO, its electron affinity can vary by as much as 1.0 eV. In this case, depositing In_2O_3 on ITO as a buffer, in addition to the typical performance improvements associated with buffers, it also results in eliminating the barrier between CdS and ITO, most likely by modifying the surface properties of ITO. As the results in Fig. 9 suggest, variations in the thickness of In_2O_3 (25-200 nm) results in devices with essentially identical characteristics; the main variations among these cells are in series resistance, but these are small and do not correlate with the thickness of In_2O_3.

In order to further evaluate the effectiveness of In_2O_3 as a buffer layer, a series of cells with varying CdS and In_2O_3 thicknesses were fabricated; figure 10 summarizes the V_{OC}'s and FF's for these cells. In general, the thickness of In_2O_3 seems to have only a minor effect on

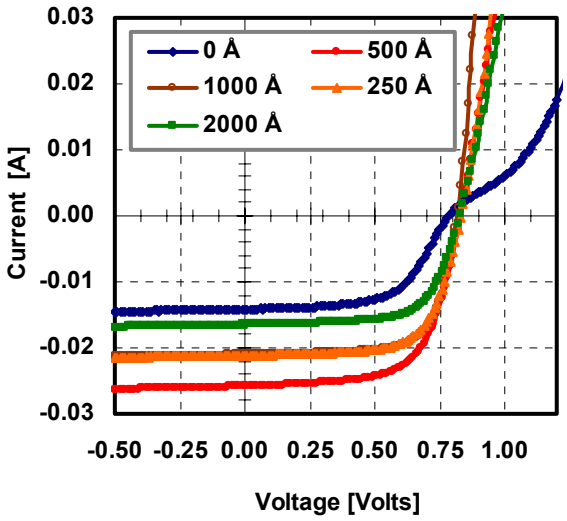

Figure 9. Light J-V characteristics for CdTe cells fabricated on ITO/In_2O_3 substrates

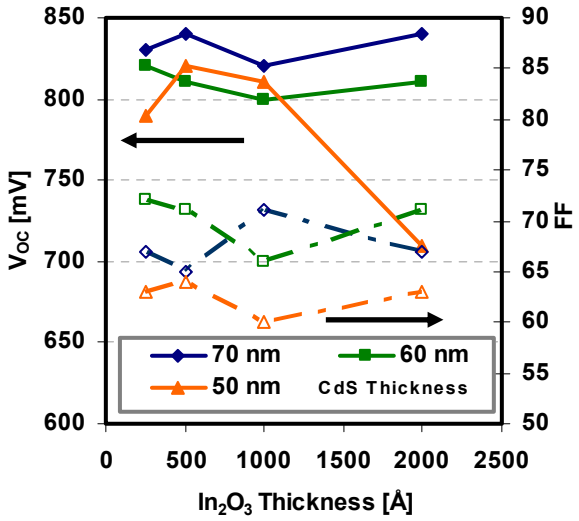

Figure 10. The V_{OC} and FF for CdTe cells fabricated on ITO/In_2O_3, as a function of the thickness of In_2O_3 and CdS

performance (with one exception); however, as the thickness of the CdS is decreased performance degrades consistently, clearly demonstrating the typical problem associated with CdTe cells, when thin CdS films are utilized. Nevertheless, In_2O_3 appears to be an effective buffer layer even at small thicknesses, and for this specific case (used with ITO), it is also beneficial in improving the contact with CdS, eliminating the rectifying behavior obtained for cells fabricated directly on ITO, by presumably affecting the O_2 concentration on the ITO surface. The light J-V and SR for the best overall devices shown in Fig. 10 are shown in Fig 11 (CdS thickness is 600 Å).

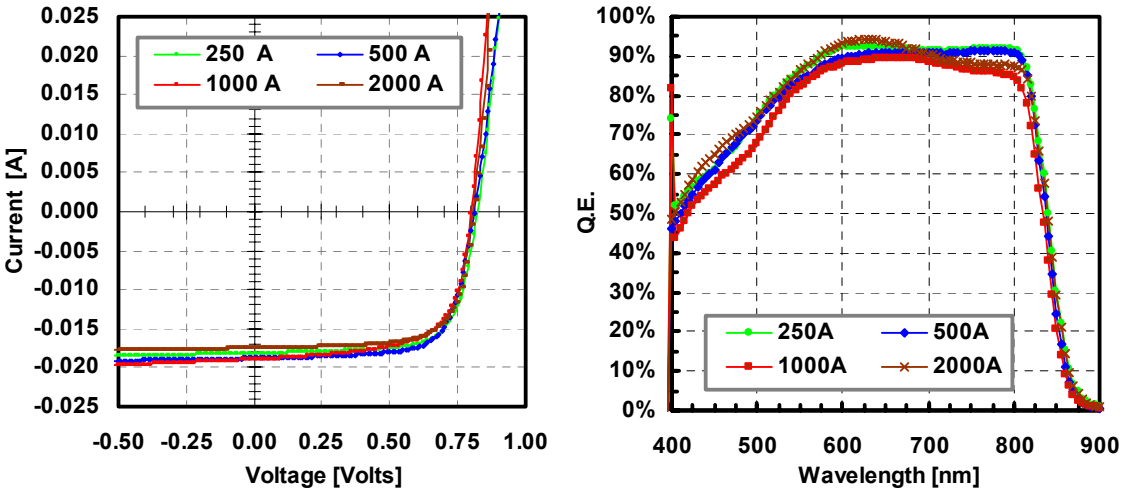

Figure 11. Light J-V and SR for a series of cells shown in Fig. 10; CdS thickness is 600 Å

4.0 Cu EFFECTS

Copper has been one of the elements mostly utilized for the formation of the back contact, and is also one of the key impurities associated with possible degradation of device performance. In an effort to improve our understanding of Cu and its influence on CdTe cells, a series of experiments were carried out where the most common approach of utilizing Cu (i.e. incorporating Cu during or immediately prior to the formation of the back contact), was eliminated from the cell fabrication process. It is well known from various SIMS studies of CdTe cells that Cu accumulates at the metallurgical junction region and in the CdS. The initial objective was to determine whether this Cu accumulation is detrimental to device performance. This work deals with two important device regions, namely the front contact (CdS) and the back contact.

4.1 Process Description

The key processing change over the baseline process, was the fact that Cu was not introduced intentionally during the back contact formation process (see Fig. 12 – left), it was however added to the CdS following the deposition of this layer (see Fig. 12 – right); no Cu was intentionally added at any other processing step; devices processed this way will be referred to as *"CuCl-treated"* cells. The CdS films were deposited by CSS [5]. The back contact was either undoped graphite, or Sb_2Te_3/Mo deposited by sputtering.

Copper was incorporated in CdS using a simple dip in a CuCl solution; the solution concentration and dip time were used as means of varying the amount of Cu. In addition to the solution approach, Cu was also deposited onto CdS by sputtering; a short-coming of this approach was the difficulty in controlling the amount of Cu as precisely as with the solution/dip method. The smallest amount that could be controlled by sputtering was approximately 10 Å. However, device results for cells processed this way suggested that even at this range of thicknesses, the amount of Cu was excessive. No device results are presented for Cu sputtered onto the CdS in this report, as in all instances the performance was extremely poor; one key limitation of these cells was poor collection as indicated by SR measurements. Results for the solution method focus on solution concentrations in the range of 10^{-7} to 10^{-9} M, as this was found to be the "optimum range".

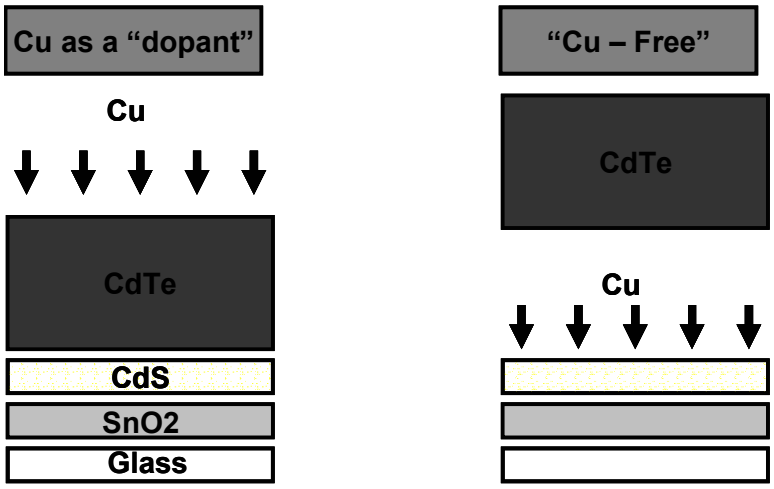

Figure 12. The baseline cell fabrication sequence (left) where Cu is added during the back contact process, and the approach utilized for the devices discussed in this section (right)

4.2 Undoped Graphite Contacts

This section discusses devices contacted with undoped graphite (used as-received from the supplier). One of the first parameters studied was the solution concentration. Table 2 lists the performance characteristics for several CuCl-treated cells; the solution concentration was varied over the range indicated. It is apparent that performance is affected by the amount of Cu introduced in CdS (assuming the amount increases with the CuCl solution concentration). The performance data obtained are very close to state-of-the-art values in particular for V_{OC}. It is noteworthy that introducing Cu directly into the CdS film (and more general in the junction region) is not necessarily detrimental to device performance; rather based on these results, it appears that a certain Cu concentration is actually necessary in order to improve device performance. The other important finding is the fact that the back electrode for these cells is "Cu-free"; however, it should also be noted that both the $CdCl_2$ heat treatment as well as the graphite itself could contain enough Cu to increase its concentration at the surface of the CdTe; therefore the term "Cu-free" implies no intentional Cu added. Reproducibility of the results shown in table 2 was satisfactory, and the concentration in the 10^{-8} M range was selected as the "optimum" for most results discussed in this report.

Table 2. The effect CuCl solution concentration on solar cell performance

CuCl Concentration [M]	V_{OC} [mV]	FF [%]
6.0×10^{-9}	766	60.1
3.0×10^{-7}	772	59.8
6.0×10^{-8}	830	67.4
6.0×10^{-7}	733	53.0

Table 3 lists device performance results obtained using the optimum solution concentration from above and varying the treatment time. The observed trends are similar to those of table 2 again suggesting that a certain Cu concentration is necessary for optimum characteristics, while "excessive" or "not enough" Cu (at this time no quantitative data is available) could be detrimental. A complicating factor in this work was the reproducibility in the CdS thickness. The CdS CSS process (in particular when O_2 is used during the deposition) exhibits a rather dynamic deposition range (it initially decreases from run to run) due to what is believed to be changes in the source material.

Table 3. The effect CuCl-treatment time on solar cell performance

Time [min]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]
5	710	55.5	23.9
10	830	66.3	23.4
15	830	65.3	23.9
20	650	48.0	19.6

The light J-V and SR for the cells in table 3 are shown in Figs 13 and 14. None of the J-V exhibits signs of a back contact barrier, suggesting that the Cu-free back contacts are possible. The best two cells (10 and 15 min) have the same CdS thickness which is also the thickest among the group. Although this may suggest that the poor J-V characteristics shown in Fig. 13 are solely due to variations in the CdS thickness, this is not believed to be the case here, as it will be shown later for samples with very similar thickness in CdS. It should be noted that the most important SR characteristic in Fig. 14 is the one for the device treated for 20 min. This cell clearly exhibits significant collection losses; this type of behavior was displayed by nearly all cells fabricated with Cu sputtered onto the CdS; in those instances, the response was even

lower. It is believed that the amount of Cu incorporated in the devices by sputtering (directly onto the CdS surface), it was always in excess, which is the reason for the poor device results obtained in those cases. Another difference between the two approaches, sputtering vs. the solution method, is the mechanism by which Cu is incorporated in CdS. During the solution method a reaction takes place and Cu is chemically bonded to S, which is not true for sputtering. This may be an important difference affecting the activation of Cu, and therefore influencing device performance.

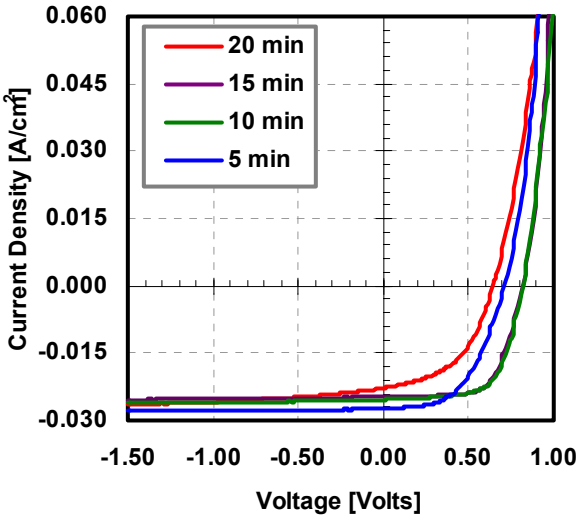

Figure 13. Light J-V characteristics of the cells listed in table 3

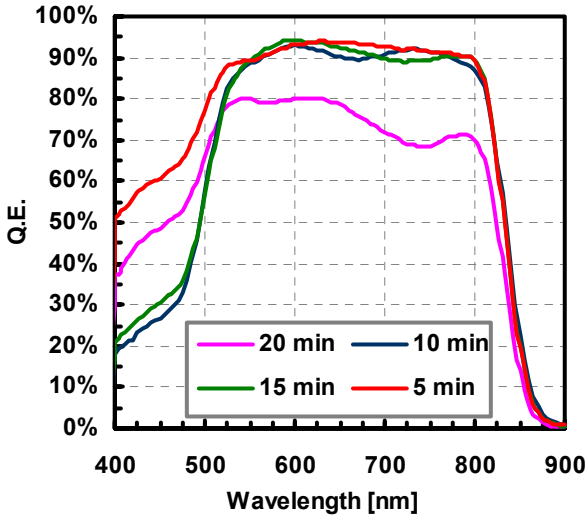

Figure 14. The SR of the cells listed in table 3

4.3 Sb_2Te_3/Mo Sputtered Contacts

In previous reports efforts to develop Cu-free back contacts included work with Sb_2Te_3. It has been indicated that this particular approach did not produce the desired results - as reported by other groups [6]; performance was always limited due to significantly low V_{OC}s and FFs; J-V characteristics always indicated that a barrier was present at the back contact, while reproducibility was always a concern. In order to further validate the role of Cu and its importance in improving device performance as described in the previous two sections, a series of CuCl treated cells were fabricated using Sb_2Te_3 as the back contact material; following the Sb_2Te_3 deposition, a Mo layer (approx. 0.5-1.0 µm) was deposited onto Sb_2Te_3.

Table 4 lists the results for a series of CuCl-treated devices, contacted with Sb_2Te_3/Mo. The CuCl solution concentration was in the 10^{-8} M range (see table 2). The performance demonstrated in these data, especially for the cells treated for 10 and 15 minutes, is the best achieved for Sb_2Te_3-contacted cells at our lab (highest V_{OC}'s and FF's). Representative light J-V for each condition listed in table 4 are shown in Fig. 15. In all cases the J-V behavior in the 1st quadrant suggests the formation of a back barrier; it is notable that the observed roll-over occurs in the 1st quadrant limiting its negative impact on the FF. The roll-over in the J-V for the 2 samples treated for 5 and 10 minutes (the two shortest times) occurs at significantly lower currents than the other two; the Cu incorporated into CdS is expected to diffuse throughout the entire device, and these results seem to suggest that "Cu-doping" of CdTe may be influencing the observed roll-over. It is also evident from the light J-V data that the shunt resistance for the

cells treated for the two longest times, is significantly lower and appears to be the main reason for the observed decrease in the FF.

Table 4. Performance of CuCl-treated solar cells, contacted with Sb_2Te_3

CuCl Treatment Time [min]	Sample #	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	Eff. [%]
5	8-6-2B1-a	760	62.30	22.00	10.42
	b	760	64.00	20.81	10.12
	c	750	61.60	21.00	9.70
	d	750	57.50	21.00	9.06
10	8-7-1A1-a	730	60.60	21.00	9.29
	b	770	71.10	20.37	11.15
	c	780	69.10	21.00	11.32
	d	780	67.00	21.00	10.97
15	8-6-1B1-a	750	53.80	23.00	9.28
	b	740	61.20	23.00	10.42
	c	720	64.70	19.04	8.87
	d	660	51.70	23.00	7.85
20	8-7-1B1-a	750	79.90	22.00	8.23
	b	780	55.00	20.83	8.94
	c	780	54.40	21.00	8.91
	d	650	41.80	20.00	5.43

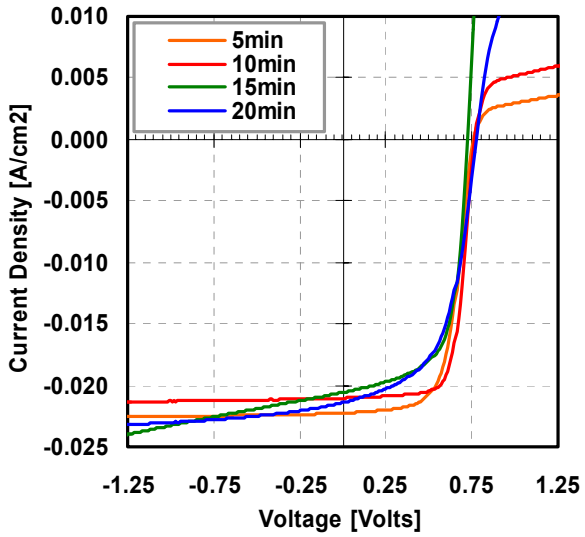

Figure 15. Selected J-V for devices listed in table 4

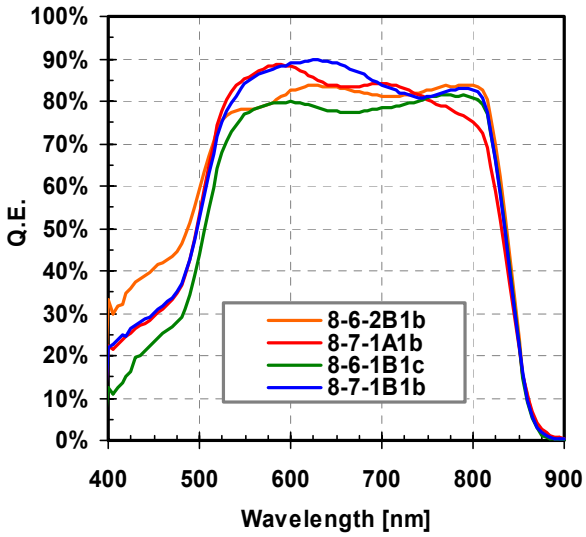

Figure 16. SR for the cells shown in Fig. 15 (table 4)

The SR for the same devices is shown in Fig. 16. The CdS thickness for all these cells is similar and relatively large, suggesting that the device characteristics observed are not influenced by the CdS thickness, but rather the variations in performance are due to the CuCl treatment and the amount of Cu introduced in CdS.

In summary, the results described in the above sections of this report, suggest that the often observed Cu accumulation at the CdTe/CdS interface, may not be a performance limiting factor.

On the contrary, these results clearly suggest that a certain amount of Cu is necessary, below which device performance decreases. It is therefore suggested that the use of Cu during the back contact process, is actually important in that it also affects the properties of the CdS, leading to improved performance. The CuCl-treatment process is believed to be an effective way to incorporate Cu in CdTe cells prior to the completion of high temperature processing, and eliminating the use of Cu during the back contact formation step. Figure 17 displays a set of light J-V data that compares a baseline device with two cells contacted with undoped graphite, one of which has been CuCl treated; the benefits of the CuCl treatment are once again evident.

At this time no information on the type of defects Cu is responsible for (in CdS or at the CdTe/CdS interface); understanding the process of Cu-related defect formation, is an important step toward developing the right fabrication processes and designing the CdTe cell, for optimum performance and stability.

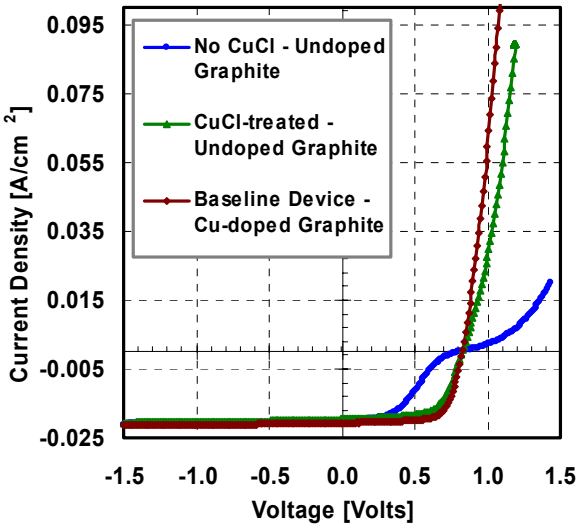

Figure 17. A comparison of light J-V data demonstrating the importance of the CuCl treatment process described in this section

5.0 BACK CONTACT PROCESSING

This section discusses device results for CdTe solar cells fabricated without the use of the typical wet chemistry etch; most effective back contact processing schemes often utilize a surface modification/cleaning step. The baseline process for USF cells includes a Br_2 etch (Br_2/methanol 0.01% vol.; 5-10 secs), prior to the application of the doped graphite electrode. As part of the efforts to investigate alternative options more suitable for manufacturing, the potential of dry etching (rf plasma) as a surface cleaning step was investigated.

Following the $CdCl_2$ heat treatment, the cells were ultrasonically rinsed with methanol to remove CdCl2 residue from the surface. After drying they were exposed to a N_2 or Ar plasma, in a March CGM 100 Plasmod rf sputter etcher; the system has a cylindrical geometry, but the sample size was small enough (2x3 cm^2) to assume that the entire area was sputter-etched uniformly. In some cases O_2 was also added to the gas mixture to determine the tolerance of the process to this gas. The process was optimized for pressure, rf power, and duration.

5.1 Sputter Power and Time

The V_{OC} and FF for a series of cells for which the CdTe surface was sputter etched using different power levels and for different times are shown in Fig. 18; the sputter gas for these devices was N_2, and the pressure was 250 mTorr. From these data it is evident that a plasma power of 50W (on average) provides the highest V_{OC}, which progressively decreases as the power is increased. The V_{OC} is also influenced by the etch time, in that at lower power levels it improves (slightly) with time reaching a maximum for a 10-15 minute etch time. At higher powers (100 W) it deteriorates with the time of etch. The effect of sputter power on the FF appears to be similar to that of V_{OC}, although the changes in the FF are significantly larger. The observed behavior is believed to be a reflection of the back contact properties. This behavior is illustrated by comparing the effect of etching time at 50W on the J-V characteristics of the solar cells (see Fig. 19). The improvement in FF initially with the etch time is due to improved contact characteristics with time. The reduction in the FF is due to the onset of rectification observed in the J-V curves of Fig. 19 for times longer than the optimum range (10-15 min). The onset of rectification at the back contact is better illustrated in Fig. 20, where the light dynamic resistance (i.e. dV/dJ [Ω-cm^2]) is shown in the range of 0.5 – 1.25 Volts. The resistance of the devices shown, initially decreases with time (from 5 to 10 minutes), but increases monotonically for the two longest times of 15 and 20 minutes. The inflection point in the dynamic resistance of the device etched for 20 minutes (marked by arrow) clearly indicates the formation of a non-ohmic back contact (i.e. the presence of a barrier). To a lesser extent this behavior is present for the device etched for 15 minutes. This overall characteristics and trends are similar to what was obtained for the devices sputter-etched at 75 W; in that case however (as indicated in Fig. 18) the FF's were lower than the devices sputter-etched at 50W; it also appears that the optimum sputter

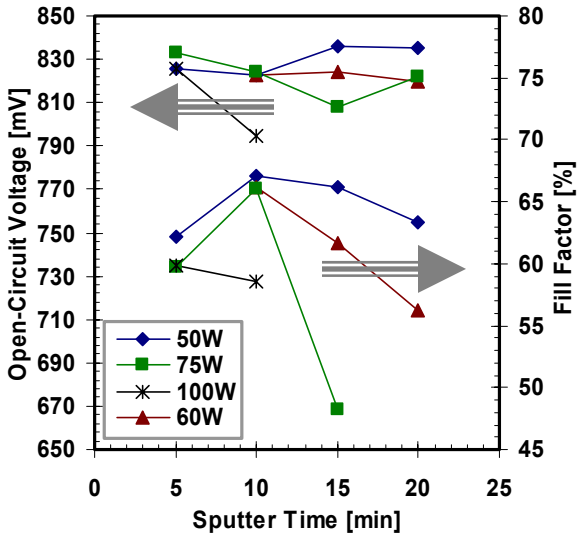

Figure 18. The V_{OC} and FF for CdTe cells sputter etched under different conditions of rf-power and sputter time

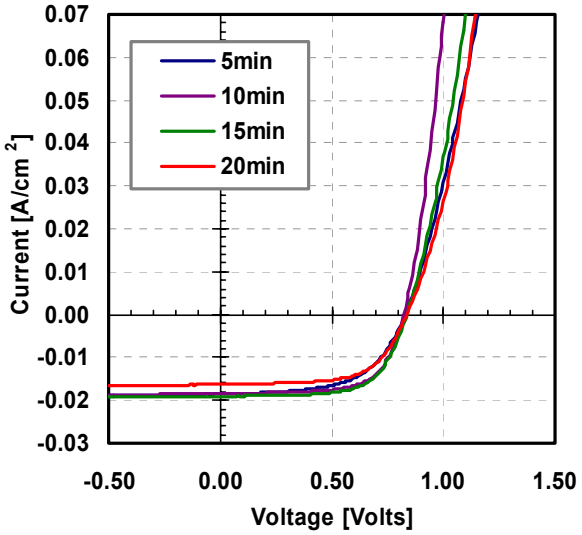

Figure 19. Light J-V characteristics of cells sputter etched at 50 W for different times

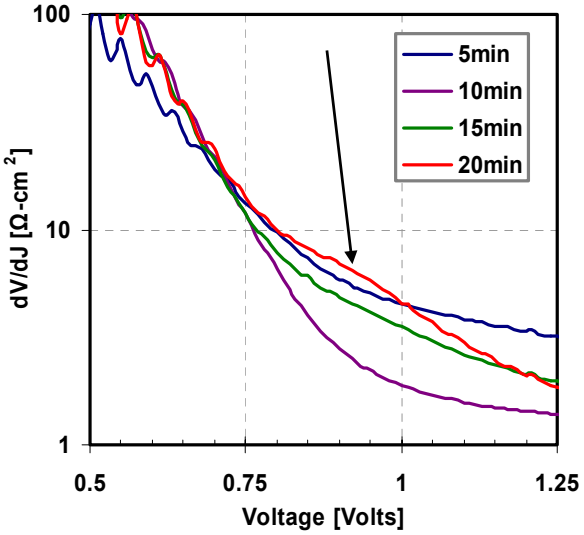

Figure 20. dV/dJ for the light J-V characteristics shown in Fig. 19

time range, decreases with power making the performance more sensitive to process variations under these conditions. The device sputter etched for the shortest time, exhibits the highest series resistance, however, in this case the dV/dJ data do not suggest the formation of a barrier at the back contact.

5.2 Sputter Pressure

The effect of the total gas pressure during the sputter etch process was also studied; the sputter power for the experimental results discussed in this section was 50 W (identified as the optimum power level based on the results discussed in the previous section), and the sputter gas was N_2. Solar cell results are tabulated in table 5. These results suggest that the effect of the etch pressure on V_{OC} is rather small and insignificant, as in all cases the V_{OC} was in the 810-830 mV range. This is not true for the FF which is in the mid 50's for the highest pressure and only 61% for the lowest. The cause for the observed decrease in the FF can be deduced using the comparison of light J-V curves of devices etched at 250, 300 and 400mT shown in Fig. 21. It can be seen that the slight reduction in the V_{OC} and the greater reduction in FF of the device etched at 400mT is due to a softer knee in the J-V curve; this could be caused by voltage dependent collection; shunting does not affect the FF and V_{OC} in this case, as the shunt resistance based on the cells' reverse bias characteristics (around 1.5-2.0 V) is essentially the same for all cells shown in the figure.

This behavior where there exists an optimum intermediate pressure for this process can be to first order explained based on the energy of the ions. At higher pressures the collision probability increases leading to lower ion energy and therefore the CdTe surface is not effectively cleaned. At the other extreme, at low pressures the ions can impinge the surface with much higher energy leading to surface damage, and compensation which can possibly damage the CdTe leading to poor collection of deeply generated carriers (i.e. a voltage dependent photo-generated current). This is just speculation at this time and additional studies/analysis are necessary to validate this model.

Table 5. The Effect of Etch Pressure on Solar Cell Performance

Etch Pressure [mTorr]	V_{OC} [mV]	FF [%]
150	831	60.6
200	826	61.6
250	823	67.1
300	819	66.5

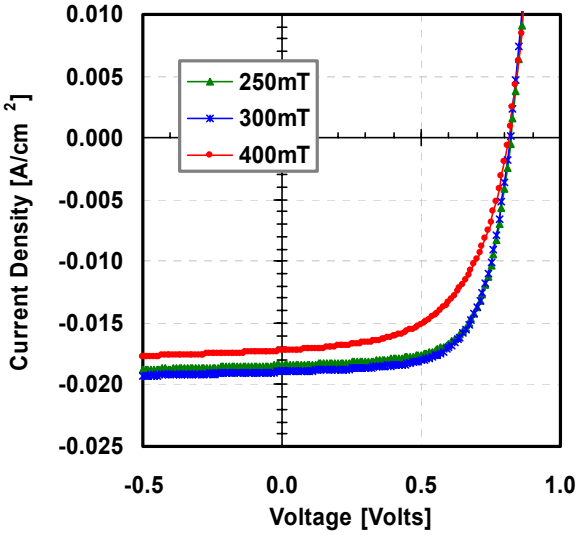

Figure 21. Light J-V for CdTe cells sputter etched at different N_2 pressures

5.3 The Effect of Ambient

5.3.1 Sputter Gas: Ar

The above described results were obtained using N_2 as the sputter gas. A series of experiments were also carried out in pure Ar as well as in a mixture of N_2 and O_2. For experiments with Ar the pressure was maintained at 250 mTorr. The light J-V for several cells sputter-etched at different power levels are shown in Fig. 22. The general trends observed with N_2 were found to hold true in this case also. As the power decreases device performance improves mainly due to improvement in the characteristics of the back contact; at low power levels no back barrier forms leading to improved FF's (while high at high power, the presence of a back contact barrier is evident in the light J-V). In this case however, the improved contact properties are obtained at lower power levels than the ones required for devices sputter-etched in N_2. This behavior as well as the results previously described (in Fig 18 and table 5) can be explained using the same model: there exists an optimum set of conditions where the sputtering process results in a clean CdTe surface free of oxides (assumed to be there as a result of the $CdCl_2$:O_2 treatment). Conditions of low power levels, short etch times, and high pressures do not result in effective oxide removal/surface cleaning, and therefore the conditions for the formation of an ohmic back contact are not optimum. At the other extreme, high power levels, long etch times, and low pressures are conditions that can cause significant damage to the surface of the CdTe, due to high energy ions or prolonged exposures to the plasma. A

damaged surface region can be heavily compensated leading to low effective acceptor levels and therefore non-ohmic contacts; it can also affect collection of deeply generated carriers (depending on the extent of the damage).

At this time it is assumed that material removal from the CdTe surface (i.e. native oxides and CdTe) is not preferential, therefore it is assumed that a Te-rich surface is not formed; however, this too needs to be verified by carrying out surface analysis.

5.3.2 Sputter Gas: N_2:O_2

Another series of experiments where performed where O_2 was added to the sputter ambient. The amount of O_2 was from varied from 0 up to 50% (while maintaining the total pressure constant at 250 mtorr). Due to equipment limitations the smallest amount of O_2 that could be controllably introduced in the sputter chamber was 4% (i.e. 240 torr N_2 + 10 torr O_2). Figure 23 shows the light J-V for solar cells processed in this manner. In all instances the use of O_2 has caused a decrease in the FF. A series resistance increase, as seen in the slope of the J-V in the first quadrant, is one of the reasons for the decrease in the FF; collection losses may also be responsible. At the highest levels of O_2 the dominant effect limiting the FF is the formation of a back barrier; a surface oxide layer was visible for this set of devices (i.e. highest O_2 partial pressure) which is the reason for the formation of the barrier. The condition of the surface at the under the two conditions of lower O_2 concentrations was not studied, but apparently O_2 in those two cases did not cause the formation of a barrier at the back contact. It is therefore concluded that this process could tolerate a certain amount of O_2.

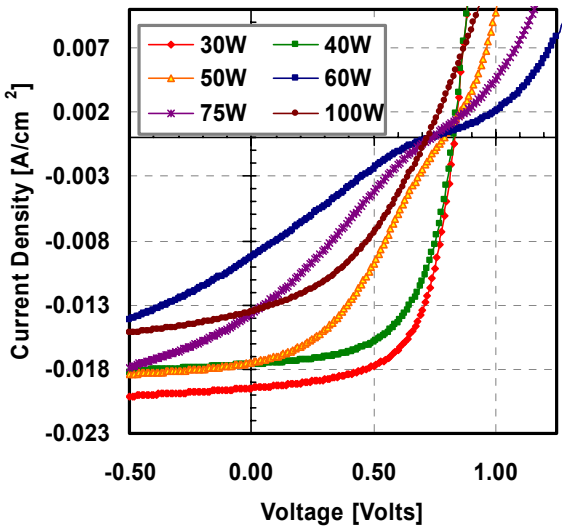

Figure 22. Light J-V characteristics for CdTe cells sputter etched in Ar at various power levels

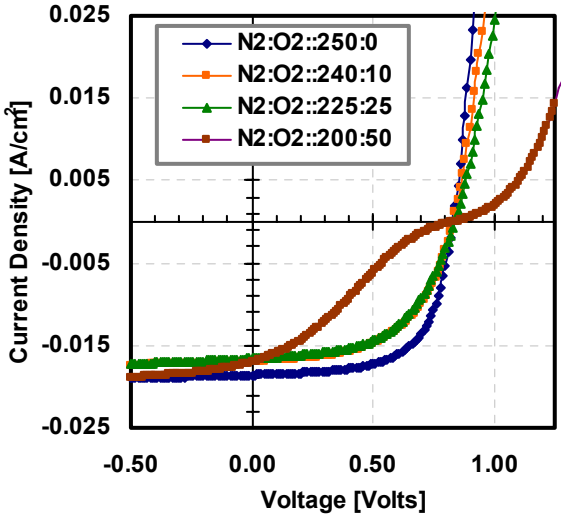

Figure 23. Light J-V for CdTe cells sputter etched with N_2:O_2 gas mixtures

Based on the performance results obtained, the sputter etch process appears to be a suitable option as a surface preparation/modification step prior to the application of the back electrode. Although, this process is no longer being investigated, future work could focus on better understanding the effect of sputter etching on the CdTe surface (i.e. stoichiometry).

6.0 COLLECTION IN CDTE DEVICES

6.1 Dependence of FF on Wavelength

The effect of "collection" in CdTe is often not taken into account in device analysis. The most prevalent device parameters used to characterize solar cells are the series and shunt resistances R_S and R_{SH}, the diode factor "A" and J_O. Collection losses affect mostly the FF, although the V_{OC} is also affected. Not accounting for collection losses can lead to erroneous results when calculating parameters such as the diode factor A.

Figure 25 displays a series of monochromatic I-V curves for a typical CdTe cell (left), and the FF as a function of wavelength for two typical devices (right). The monochromatic I-V data was collected using interference filters with a bandwidth (BW) of approximately 20 nm. Using data from SR measurements the light intensity for each wavelength was adjusted to produce the AM1.5 equivalent current at the specific wavelength (within the 20 nm BW). The monochromatic I-V shows similar slopes (i.e. dV/dJ) at reverse bias, suggesting that R_{SH} does not affect the FF; nevertheless the 4th quadrant behavior clearly demonstrates a considerable "softening" of the knee of I-V as the wavelength increases. This is interpreted to be the result of inefficient collection at the longer wavelengths, since at these wavelengths photogeneration extends deeper into the device, and carriers have a longer distance to travel before they are collected. The FF as a function of wavenelgth for two typical solar cells is also shown in Fig. 24, where the wavelength dependence of the FF is demonstrated. The AM 1.5 FF for both cells is also marked, and as seen in the figure, it lies between the two extreme values of the monochromatic FF's. Based on these results it is suggested that the FF in CdTe cells is affected by collection losses (in addition to the R_{SH} and R_S limitations).

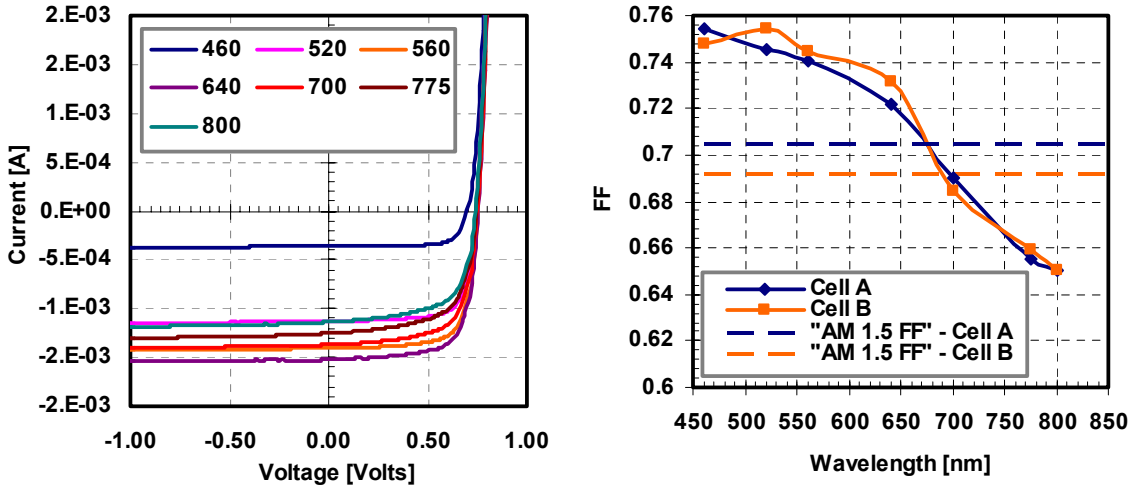

Figure 24. Monochromatic light I-V data for a typical device – left; the FF as a function of wavelength for two typical CdTe cells - right

6.2 Collection Function Estimation

In order to study the effect of collection losses the collection function (H(V)) was estimated using monochromatic I-V data (similar to those shown in Fig. 24). Figure 25 shows the estimated collection for several wavelengths. In order to obtain these collection functions the assumption

was made that for 520 nm light, collection is voltage independent (i.e. J_L is constant and not a function of voltage). As the data suggests, the longer the wavelength, the greater the effect of the collection function is. All collection functions were determined up to V_{OC}. Figure 26 shows a polynomial fit to two of the data sets shown in Fig. 25; namely the collection functions for 640 and 700 nm. It should be noted that these are simple mathematical fits of the measured data, and are not based on a physical model. For this particular case these two wavelengths were chosen to represent an "average" collection function, based on the FF dependence shown in Fig. 24, where the AM 1.5 FF lies between the FF for 640 and 700 nm.

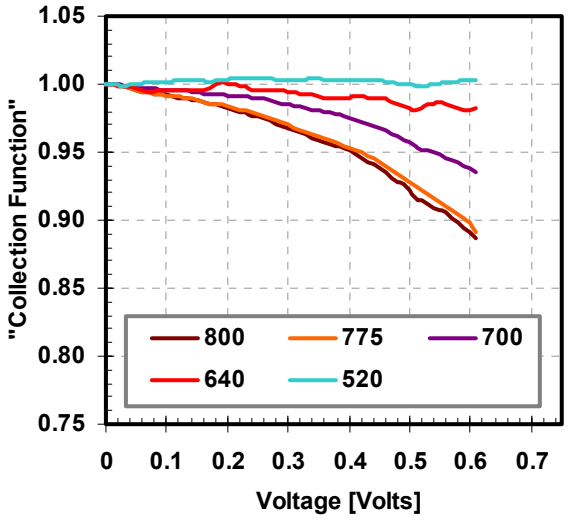

Figure 25. Collection functions estimated from monochromatic light I-V data

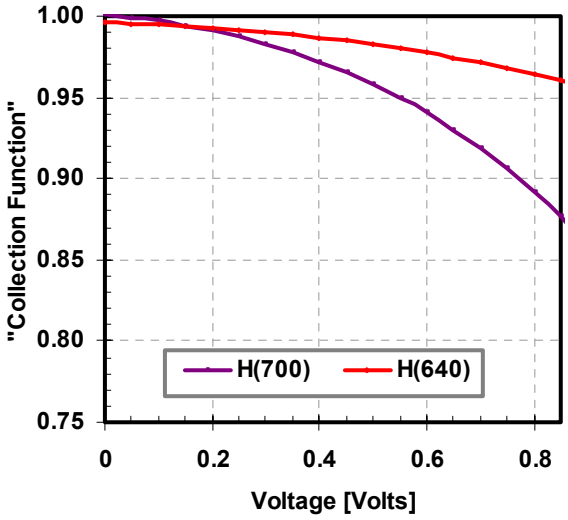

Figure 26. Polynomial fits for two of the collection functions shown in Fig. 25

6.3 Effect of Collection on Device Parameters

Using the pair of A and J_O values listed in table 6, the light J-V for an ideal solar cell (assuming constant J_L) are plotted in Fig. 27. In the same figure the effect of the light J-V for two cases where the collection function is taken into account is also shown; instead of assuming a constant J_L, the collection functions shown in Fig. 26 were used for the simulations (i.e. J_L x H(700) and J_L x H(640)); the collection functions were only applied to the fourth quadrant characteristics. The calculated loss in FF due to the collection losses is shown in table 6; the FF loss for the collection function H(700) is significant and on the order of 10%.

Finally, Fig. 28 shows the calculated light A-factors as a function of voltage for the three devices of Fig. 27; as noted above, these J-V characteristics were generated assuming a constant J_L for the ideal device, and the two collection functions of Fig. 26 for the other two. The calculated A-factors in Fig 28 ignore collection losses and in all three cases assume a constant J_L (what is typically done when calculating light A-factors). As expected the "ideal" case results in an A-factor of 1.6. However, due to the fact that collection losses were ignored, the A factor for the other two devices is significantly affected, and it only approaches the value of 1.6 at voltages above V_{OC} (0.850 Volts). For real devices this voltage region is often affected by resistive losses. This analysis clearly demonstrates that calculations of the diode factor A assuming no collection losses (i.e. constant J_L) can easily lead to overestimating this device parameter.

Table 6. Fill factor losses using the collection functions estimated in Fig. 26

	"Ideal"	H(700)	H(640)
J_O [A]	1.00E-11		
A	1.6		
J_L [A]	0.025		
V_{OC} [mV]	850		
FF	*83.3%*	*74.9%*	*80.8%*
FF Loss (%)		*10.08%*	*3.0%*

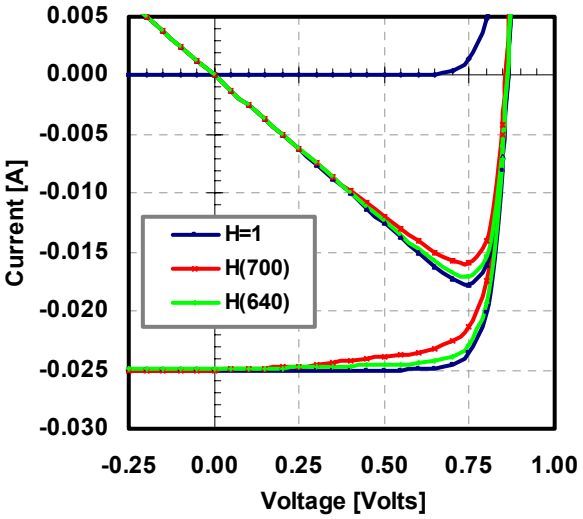

Figure 27. Light J-V data for an ideal device (H=1) and for two devices with collection losses, using the collection functions of Fig. 26

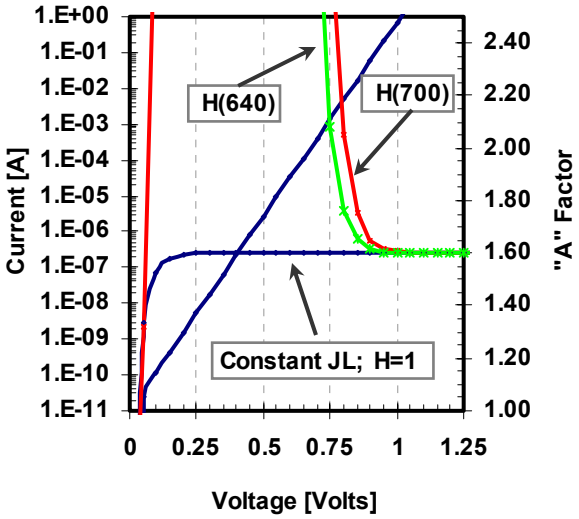

Figure 28. The calculated light A-factors for the data of Fig. 27

PART II – CIGS

1.0 INTRODUCTION

During Phase I of this project the focus was on completing experiments relating to the extended capabilities of our new vacuum system. Specifically the two-chamber load-locked system was designed to eliminate Se background flux during metal deposition and provide more control of the vacuum ambient. In the Annual report for Phase I we summarized our findings relative to these new capabilities. An important and unexpected result was that elimination of Se during metal deposition significantly reduced effective Ga bonding and hence the ability to increase the band gap above the 0.95 eV fundamental CIS value. This effect was also influenced by the vacuum ambient implying a role by residual water vapor.

In parallel with our experimental studies we were also conducting AMPS©-based simulations. Those key aspect of those simulations was the use of native defects whose properties were provided by the NREL Theory Group [7]. Although use of the most prominent defects resulted in substantial agreement with experimental results, there were always some discrepancies. This combined with experimental observations that vacuum ambient was playing a role in device properties suggested that native defects were not the whole story. It was apparent that we also had to include impurities in our thinking. We already had evidence that impurities from the vacuum ambient were operative, but we also recognized the need to include other sources of impurities such as those emanating from the substrate. Clearly it is recognized that Na plays a role in device performance due to ongoing studies. While it is clear that Na plays a role, the nature of its role has not been determined, and it is likely that the operable mechanisms are influenced by specifics of the deposition process. Consequently, in Phase II of this project we decided to focus much of our effort on determining the role of impurities, particularly Na, on the properties and performance of our devices. The effort consisted of both experiment and simulation. The experimental results indicate a strong role by Na. While it is not surprising that Na plays a role, its influence is stronger than expected and interwoven with other mechanisms. Attempts to sort it all out will be presented.

2.0 EXPERIMENTAL

Since some results presented below will involve comparisons between devices made in our new two-chamber system and in our original single-chamber system it is appropriate to provide a brief description of these processes. Further details can be found in earlier publications[8]. Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 °C. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. Much of what is presented in the following discussion is for our baseline process. In this process the order of deposition of the precursors is Cu/Ga/(In + Se). Deviations from this procedure will be presented as they arise in the ensuing discussion. Formation of the semiconductor layer takes about one-half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by sputter deposition of high ρ/ low ρ ZnO. In our original single-chamber system the elemental sources were located to give rise to compositional gradients to enrich the data base. To get as much mileage as possible out of a run we fabricate 5 x 5 arrays of 0.1 cm^2 devices by using a shadow mask for the ZnO deposition. The arrangement of sources around the substrate is shown in figure 1.

In the two-chamber system the compositional gradient is smaller for stationary deposition and can be largely eliminated by movement of the substrate during deposition. Background moisture can be significantly reduced by use of the load lock. The effect of this on performance was addressed substantially in Phase I and the results presented in the Phase I reports. A key aspect of the design is the ability to deposit the precursor metal layers in the absence of background Se flux. In addition to these targeted design advantages the two-chamber system has significantly improved control over deposition rates and substrate temperature profiles.

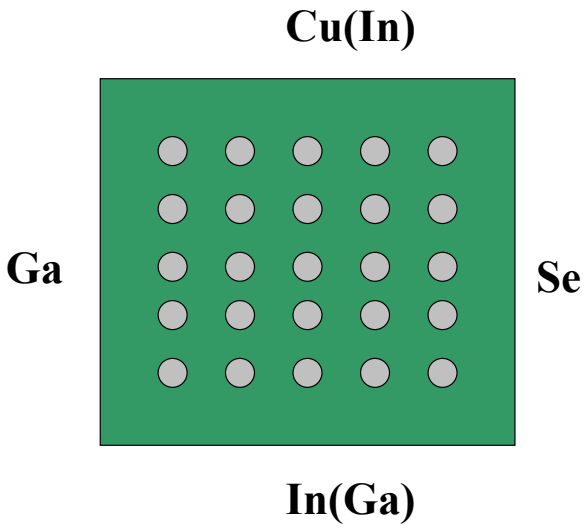

Figure 1. Arrangement of sources around the 2" x 2" substrate for the original chamber. For the new chamber Cu and Se are uniform, and the sides of highest In and Ga composition are shown in parentheses.

In light of the experiments involving Mo it is also appropriate to provide further details of our Mo deposition process. The deposition chamber is a turbo pumped load-locked chamber with provisions to preheat the glass substrate in the load lock. Mo is deposited from a 4-9's pure target using DC magnetron sputtering. In our standard process a first Mo layer of about 300 nm thickness is deposited at about 2 mTorr of Ar. The low pressure is found to aid adhesion of this layer to the glass substrate. A subsequent layer of about 700 nm is deposited at a pressure of 5 mTorr. Typical target voltage for the 3" diameter magnetron is 400 volts. As will be discussed below, Mo properties are dependent on each of these parameters and as they are varied, overall device performance is affected. The influence of Mo deposition parameters on performance, in fact, is found to be surprisingly strong.

3.0 RESULTS AND DISCUSSION

3.1 Native Defects and Compensation

In our earlier efforts much of our device modeling was based upon assumed dominance by deep levels[9]. This resulted in good agreement with experimental results and to some extent helped point the way to new wrinkles in processing. However, as we all know, models that fit a set of data are rarely unique, and in this case we did not know what the deep level was that we were using as the basis for modeling. Materials modeling by the NREL Theory Group is assisting these efforts by providing insights to likely defects in CIGS[7]. In Quarterly Report 5 of year 3 in the predecessor to this project we presented modeling results based upon use of the primary defect levels identified by the NREL Theory Group. The defects with the lowest formation energies are the V_{Cu} and the M_{Cu} + $2V_{Cu}$ defect pair. The V_{Cu} is acceptor-like, and the defect pair is donor-like. Both are shallow, and thus compensation effects are operative. (A full discussion of this can be found in the earlier report). What we want to pick up on here is the result that indicated a difference in dark IV curves when one or the other of these defects is dominant. In figure 2 we show an extended version of that result. The lines are simulations for varying levels of compensation. The lowest lying line is the ideal case of no defects. The device band gap is 0.95 eV, so with an expected Jsc of 40 mA/cm^2 extrapolation of the dark IV would

result in an expected Voc of 600 mV. The solid line is the dark IV that results from fitting the power curve of one of our top-end devices. To fit the data for these devices requires about 40% compensation. The top-most line is for full compensation, and the one below it is for 80% compensation. As can be seen, as the level of compensation increases, the dark IV shifts upward and thus lowers Voc. However, at the highest compensation levels there is bending over at high voltages which reduces the expected loss. Based upon these observations we feel that the dark IV may be a telltale that indicates the level of compensation, and thus indirectly suggests the operative defects.

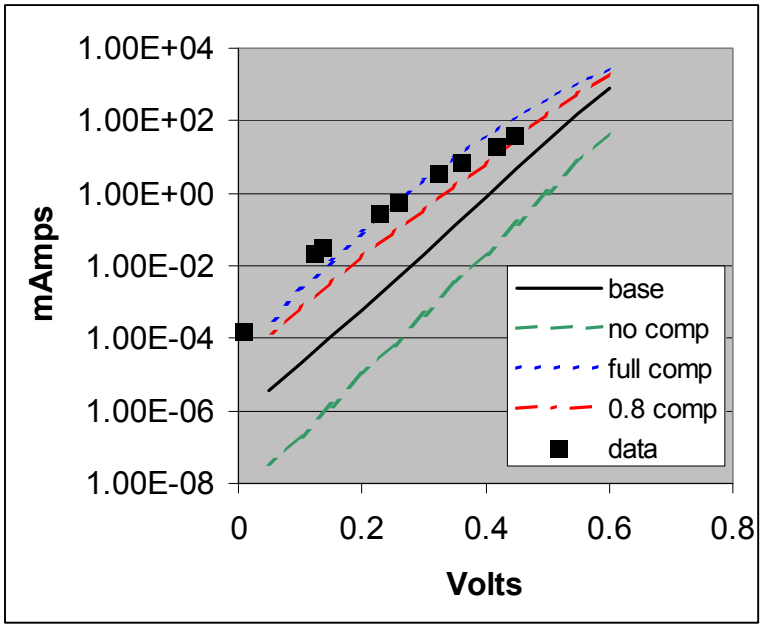

Figure 2. Simulated and experimental IV curves for devices with various levels of compensation.

Since the results in figure 2 only involve shallow levels, there is a suggestion that deep levels may not be operative as originally thought. To sort this out we are starting to look more carefully at dark IV data. The data points(□) in figure 2 are experimental data from a device with Voc of about 425 mV. The data is from Isc –Voc plots. This eliminates contributions from series resistance allowing a more direct look at junction properties. As can be seen, the data falls near the curve for complete depletion, but seems to bend over a bit more at high voltage. If the behavior is explainable only by the shallow states used for the simulations in figure 2, then it would be between 80% and 100% compensated. In figure 3 we show the simulation of the junction region for 40% and 80% compensation in simplified band diagram format. As can be seen, the space charge width increases from about 200 nm to 450 nm over this range of compensation. At full compensation, the device would be completely depleted which would result in more unusual behavior. However, 80% compensation with a space charge width of 400 – 500 nm is not unrealistic. 200 – 500 nm is typically what we observe. This model would result in a direct correlation between Voc and capacitance.

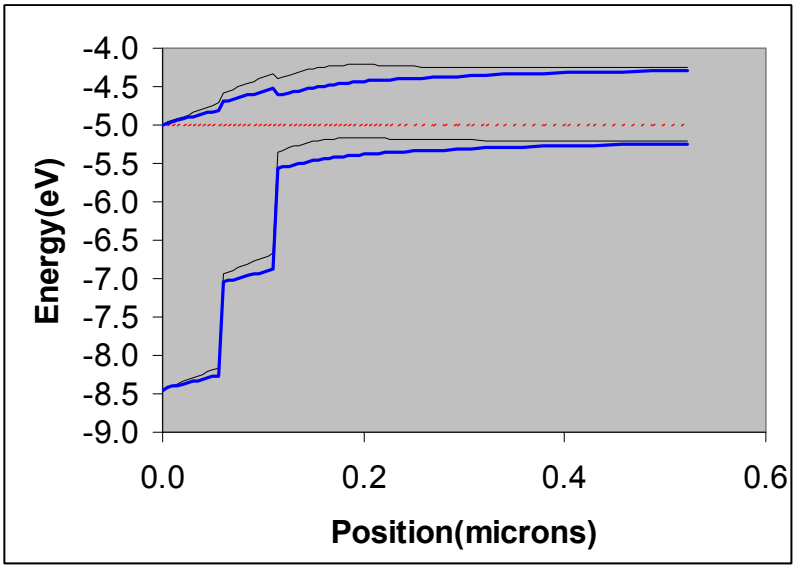

Figure 3. Simulation of junction region in CIGS for 40%(light line) and 80% (heavy line) compensation.

That is, as compensation increases, the space charge width increases resulting in decreasing capacitance and correspondingly decreasing Voc. We have observed such behavior previously in our photocapacitance studies[10], but based on the then current model were attributing it to deep states. These new observations suggest that shallow states may be playing a role as well because of their compensation effects.

It now becomes important to distinguish between contributions from deep and shallow states if we are to fully understand what is going on. The near fit of the data to the shallow state simulations is suggestive, but just a start. The bend over in the data seems to favor additional mechanisms. In particular, deep states can produce such behavior[9]. A comparison of diode factor behavior for deep and shallow states is shown in figure 4 from our earlier simulation efforts. As can be seen, shallow levels(at Ec – 0.27 eV) produce low diode factors and thus steep IV curves like those in figure 2. However, mid-gap levels produce diode factors which become large in certain voltage ranges and thus can produce the kind of bend over (small slopes) seen in figure 2. A more direct comparison can be made by observing the experimental diode factor in figure 5. This is from the data in figure 2. The behavior is seen to be much more like the mid-gap simulation in figure 4 than the shallow state simulation and thus favors contributions from deep states.

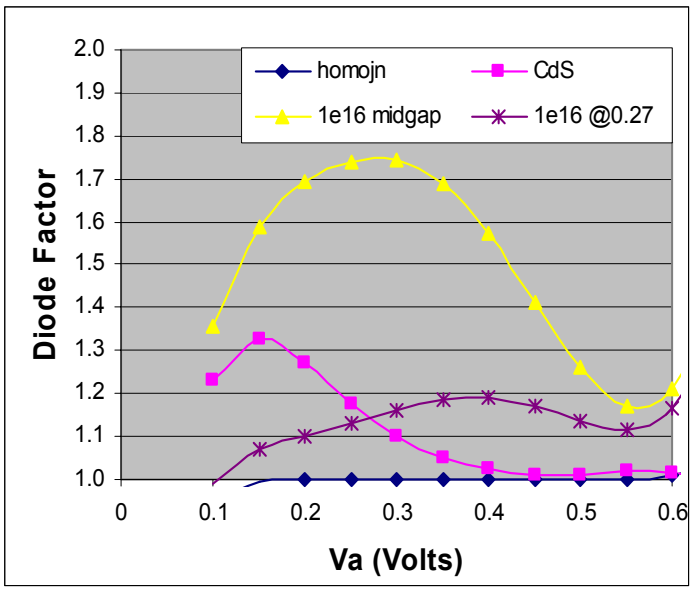

Figure 4. Simulations of diode factor for various junction configurations.

Although there appears to be support for deep state contributions in the experimental data, determining what these states might be is not straightforward. Also, our experimental results indicating that impurity contributions need to be added to our defect profile require that we first sort those out as they may be the source of deep as well as shallow levels.

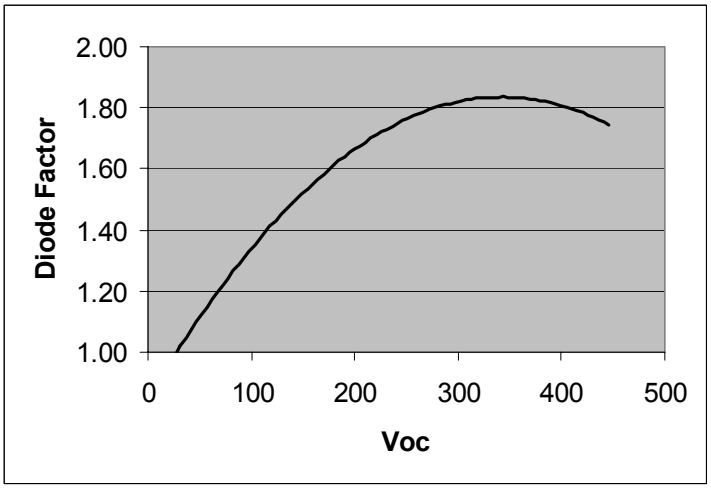

Figure 5. Experimental diode factor voltage dependence.

Before proceeding to impurity considerations we need to consider some of the criteria that have guided our approach based upon native defects. We have shown that while the V_{Cu} acceptor-like defect plays a major role, additional defects are required to match experimental observations. In particular, we have found that Voc's below 550

mV can not be simulated just by raising the V_{Cu} defect level. As the level is raised to further lower Voc, Jsc and FF are affected in ways inconsistent with experimental data. To maintain consistency and lower Voc we find it necessary to use a combination of V_{Cu} and (M_{Cu} + $2V_{Cu}$) paired donor-like defects. This is shown in figure 6 and is discussed in more detail in Quarterly Report 5 from year 3 of the predecessor project to this. The base case contains 1 x 10^{16} V_{Cu} defects in the near surface region and 1 x 10^{15} in the bulk. Adding 1 x 10^{15} and 1 x 10^{14} (M_{Cu} + $2V_{Cu}$) donor defects to these regions respectively results in a downshift in Voc as seen. Raising the level of the (M_{Cu} + $2V_{Cu}$) donor defects to that of the V_{Cu} defects in these regions results in a downshift in Voc below 500 mV while not significantly affecting Jsc and FF. Thus we have argued that compensation plays a significant role in performance, and thus it is important to understand and control it. Along these lines we need now to consider the effect of impurities, in particular that of Na in determining the overall defect profile.

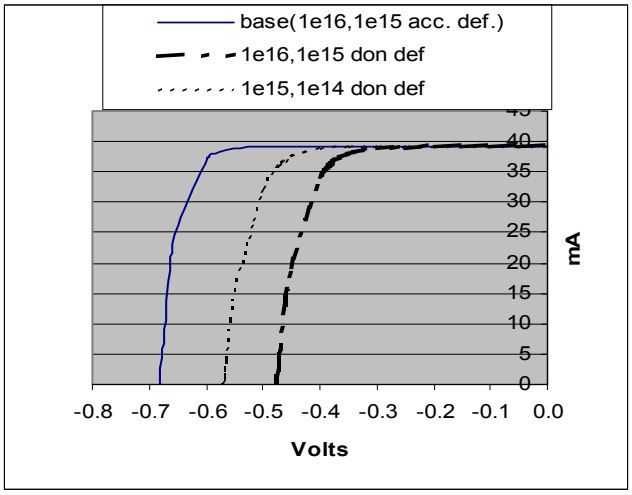

Figure 6. Effect of the M_{Cu} + $2V_{Cu}$ paired donor defect on performance.

3.2 Substrate Effects – the Role of Na – Reduced Na

Our simulation efforts to date have been driven by the formation energy of the potential defects as well as their location in the energy gap. Lacking reliable experimental values we have to vary cross sections and concentration levels to achieve consistency with experiment. Further experimental verification of these parameters would be helpful. However, there is an additional potential contributor to the defect structure that has to be considered. It is well known that Na has a significant influence on device performance. That influence includes both structural and point defect components. At this point we are particularly concerned with the latter as another potential contributor to the overall defect scenario. Na is known to migrate throughout the film and is thought to accumulate at interfaces and grain boundaries. Its role can be quite different in these two locations, so we must concern ourselves with all of the possibilities. Because its bonding tendencies do not favor tetrahedral locations, a direct substitutional role is not energetically favorable. Rather, it is thought to be more effective as a catalyst that promotes the oxidation of In at selenium vacancies [11]. The reaction can be described as follows [12]: V_{Se} can form at surface In sites. These act as donors. Oxygen at the surface in the presence of Na picks up two electrons from the lattice producing O^{2-} which then fills the V_{Se} on the In surface. The defining equations are as follows:

$$\frac{1}{2}O_2 + 2e_{cb}^- \overset{Na}{\Longleftrightarrow} \left(O_{ads}^-\right)$$

$$\left\{In_M^x - V_{Se}^{++}\right\}_{surf} + \left\{O^{2-}\right\}_{ads} \Leftrightarrow \left\{In_M^x - O_{Se}^x\right\}_{surf}$$

The superscripts denote the state of charge with “x” being neutral. The site is converted from being a donor to an acceptor as a result of the oxidation. Needless to say this mechanism

requires V_{Se} as well as O. Also, the effect of Na is observed to be stronger in Cu-poor films[13]. O_{Se} are reported to have an activation energy of 120-140 meV and can be simulated accordingly. However, our first concern here is to investigate the effect of Na on our devices experimentally.

To initiate this investigation we use Si_3N_4 barrier layers that are deposited on the soda lime glass substrate prior to Mo deposition. The barrier layers are deposited from a Si_3N_4 target using RF magnetron sputtering and range in thickness from 20 – 1600 Å. CIGS is then deposited using our standard process that produces devices with band gaps in the 0.95 – 1.0 eV range. For this round of experiments we deposited a series of samples in our old and our new deposition systems. The resulting Voc dependence on Si_3N_4 thickness is shown in figure 7. As can be seen, there is a much more rapid drop for devices made in the old system. At this point we can speculate as follows. The primary difference between the two systems is the ability to deposit Cu in a Se-free environment in the new system. In fact the new system has been designed with this specifically in mind, since we have argued that devices made in the old system are limited by the formation Cu_xSe_y of during Cu deposition. This results from the large accumulated amount of Se inside of the system and the high deposition temperature of Cu. In the new system Cu is deposited in chamber 1 which does not contain Se and then is moved to chamber 2 for the selenization step. Thus we speculate that Cu_xSe_y formed in the old chamber is not only a problem in itself, but also results in a higher level of V_{Cu}. In this environment the oxidation reaction is more prevalent, and our process has been tuned to tweak Voc according to this environment. As we add Si_3N_4, Na, the catalyst for oxidation, is reduced resulting in less oxidation and compensation, and thus lower Voc. In the new chamber oxidation is less prevalent, and the process has been tuned accordingly. Thus as we reduce Na the accompanying reduction in oxidation is less important, and thus there is less of an effect on Voc. The data point at 200 Å from the new system plot is an interesting anomaly. For this device the Cu was deposited in chamber 2 of the new system. Chamber 2 has a Se environment, though it should be less intrusive than that of the old system. Thus we might expect to form some Cu_xSe_y during Cu deposition, but less than that in the old system. This should result in a drop in Voc somewhere between the old and new system. As can be seen, that data point is below the trend line for the new system data in qualitative support of expectations.

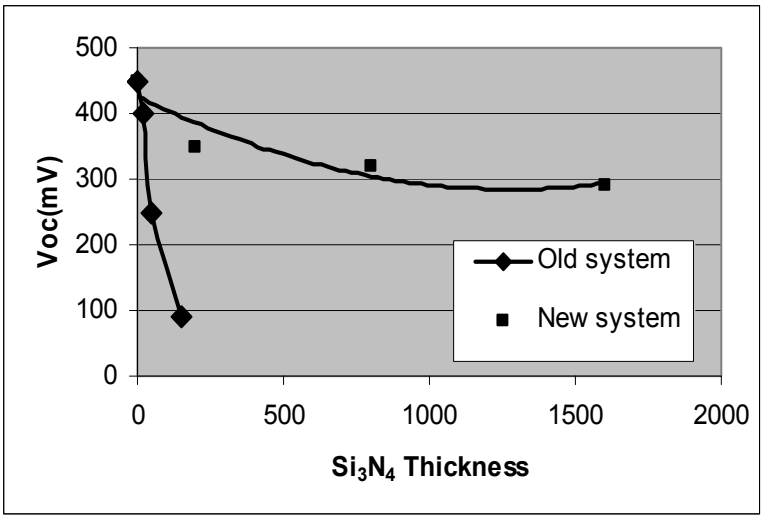

Figure 7. Voc versus Si_3N_4 thickness for a series of CIGS devices from our old and new system.

Isc data, though somewhat sketchy at this point, is shown in figure 8. The main message here is an obvious drop with increasing thickness. Correcting Voc for this drop will result in less of a drop for the new system than that exhibited in figure 7. The magnitude of the drop in Isc is interesting in that it is much stronger than usually observed in simulations. This suggests a more complex role for Na than the addition of a simple compensating defect throughout the film. More data will be required to sort this out.

To gain further insights to these mechanisms ageing data has been taken on these devices. After fabrication the devices were just stored in the lab under ambient conditions. After a period of 2- 4 months they were re-measured following light soaking and then annealed for 5 minutes at 100 C in ambient air. The results for Voc and FF for devices with a 20 Å Si_3N_4 blocking layer are shown in figures 9 and 10. These are from the old chamber with proposed higher oxidation rates. As can be seen, although the devices with the Si_3N_4 blocking layer start out at lower performance than the reference, they are much more stable. This is an interesting result that ties in with the above discussion. In the absence of a blocking layer the process is tuned to the film environment. This results in optimized initial performance. However, as the devices sit around in the presence of air and moisture, they continue to oxidize and degrade. The process is not reversible, as annealing does not help. Devices with the blocking layer are under oxidized and hence have lower initial performance. However, as they sit around, the oxidation process can continue, though at a slower pace because of the reduced Na environment. And, as seen in figures 9 and 10, their output can increase over the initial values as they oxidize. In keeping with this scenario we also point out that unlike what is commonly reported in the literature by others, our devices do not require or benefit from a post-deposition anneal. While we are just starting to scratch the surface on these complex phenomena, it is clear that substrate effects are playing

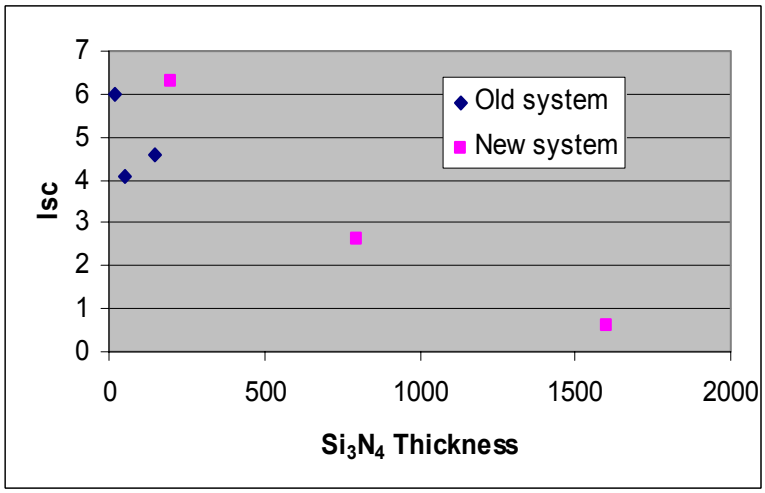

Figure 8. Dependence of Isc on Si_3N_4 thickness for a series of CIGS devices from our old and new system.

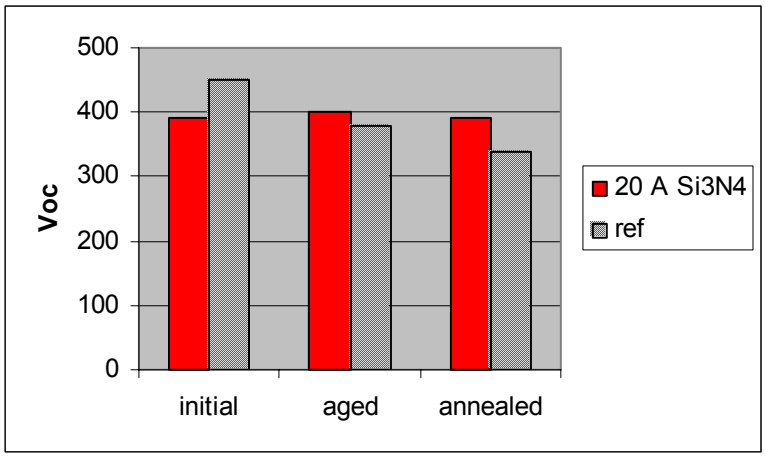

Figure 9. Dependence of Voc on ageing for devices from the old system with a 20 Å Si_3N_4 layer.

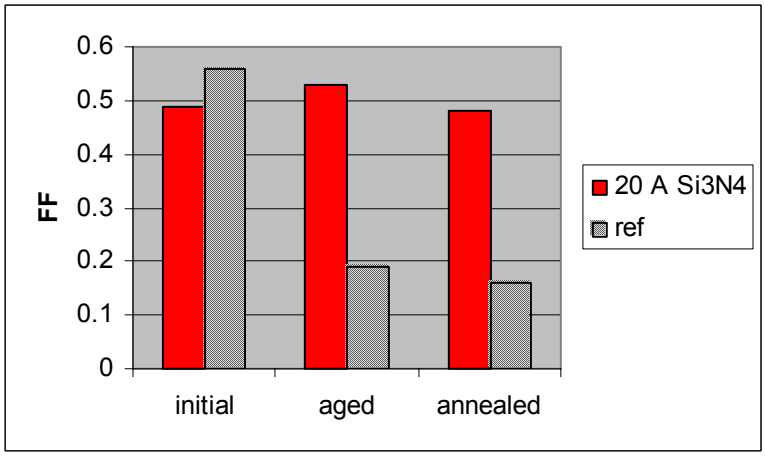

Figure 10. Dependence of FF on ageing for devices from the old system with a 20 Å Si_3N_4 layer.

a significant role in performance. In the next section we continue these studies by increasing the Na content.

3.3 Substrate Effects – the Role of Na – Increased Na

While it is convenient to add Na by depositing, for example, Na_2 Se, we chose instead to attempt modulating the Na level by varying the Mo thickness. A particular side issue that we hope to gain insights to is that every time we switch to a new batch of glass we can expect fluctuations in performance. This, of course, signals the fact that the substrate is influencing device performance. Clearly it would be advantageous to understand the underlying mechanisms and be able to control them. Ideally this would be accomplished by adjusting the Mo deposition conditions, so we wished to learn to what extent this could be done.

Our Mo deposition procedure is not unlike that commonly reported in the literature. It is deposited by RF magnetron sputtering using a 3 inch diameter Mo target. The important aspects of the deposition are that the film is a two layer film deposited at two different pressures. Our typical total film thickness is about 1 µm. About half of the layer is deposited at a high pressure of about 5 mTorr and the second half is deposited at about 1.5 mTorr. It is commonly known that the high pressure layer results in good adhesion, though has higher resistivity. The second layer is thought to be denser and have lower resistivity. The film is deposited at room temperature following preheating of the glass substrate. The preheating is done just above 100 º C primarily to dry the glass surface. However, this step as well as the entire glass cleaning procedure influences the surface Na level of the glass.

The devices for this study were deposited in our single chamber system using our baseline run conditions. Jsc values were determined by integration of QE response using Si and Ge references calibrated by NREL. The effect of Mo thickness on Jsc is shown in figure 11. There is a clear increase of 1 – 2 mA/cm^2 when the Mo thickness is reduced below the 1 µm range. We are postulating that this is at least in part due to an increase in the Na level. We have preliminary EDS data supporting that the Na increases with reduced Mo thickness, but the data is not yet conclusive. The increase in Jsc at low Mo thickness is observed to be due to an overall upward shift in the QE spectrum. We have modeled such behavior previously in terms of changes in defect levels in the top layer of the device. It is not surprising that Na may find its way there, but this result would then suggest that that region is the most sensitive to Na.

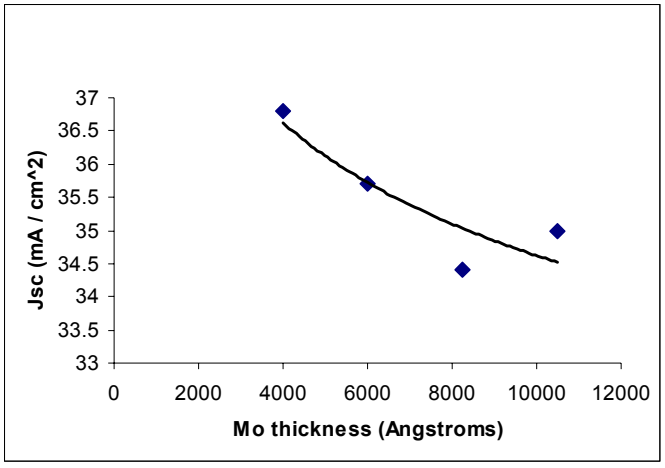

Figure 11. Jsc versus Mo thickness for standard CIGS devices.

The effect of Mo thickness on Voc is shown in figure 12. As can be seen, there is little effect down to 6000 Å, then Voc plummets. Again interpreting this result in terms of Na suggests a range of insensitivity for Voc down to 6000 Å at which point an apparent threshold is reached. The two data points below 6000 Å offer further insights. At a total Mo thickness of 6000 Å 3000 Å is deposited first at high pressure, and the remaining 3000 Å at low pressure. In reducing the

thickness further, if the thickness of the upper low pressure layer is reduced below 3000 Å, loss of adhesion sets in. The data point at 5000 Å has composition 3000 Å/2000 Å for the high/low pressure layers. The low Voc of 360 mV is thus the result of a change in stress at the Mo interface. The data point at 4000 Å has composition 1000 Å/3000 Å and is seen to have a higher Voc. The effect on Voc then is not just that associated with Na, but also includes changes in interfacial stress. Jsc seems to be less affected by stress related issues. Nevertheless, these results again show Voc and Jsc going in opposite directions with Mo thickness as the varying parameter. We have observed such behavior previously that was associated with metal ratios and defect formation, particularly in the top region of the CIGS near the CdS. We have focused a lot of effort on understanding and controlling the mechanisms that affect Voc and Jsc, and in particular have sought out means of controlling these parameters independent of each other to optimize performance. The details of our process recipe are a result of optimizing these tradeoffs. These new results with Na and stress as additional factors, provide new opportunities for further optimization.

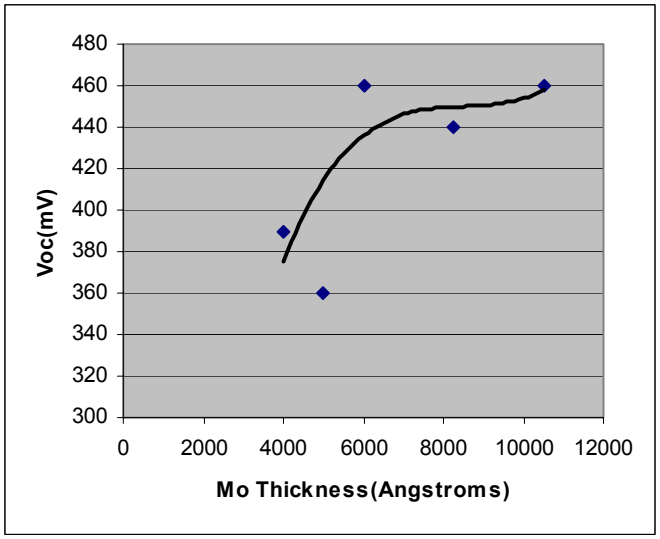

Figure12. Voc versus Mo thickness for standard CIGS devices

Based upon the above results it is now clear that Mo deposition conditions are a more critical factor than we realized. This is particularly relevant considering the nature of the Mo sputtering process. Starting with a new Mo target the sputtering environment changes continuously as the target breaks in. Consequently, a decent sputtering rate of 2- 3 Å/s for a new target requires a target voltage in excess of 600 volts, while only about 400 volts is needed for a broken-in target. Because a high target voltage can produce high energy particles that might damage the growing film, the tendency is to keep the voltage down. For a new target this translates to a slower deposition rate. Normally this might not be a bad thing because a slower arrival rate leaves more time for surface migration to lower energy locations which results in better film properties. However, this does not seem to be the case here. In figure 13 we show the dependence of Jsc on Mo deposition rate. Jsc increases with increasing deposition rate, which of course is a good result from a manufacturing perspective. It is also interesting that the Mo properties seem to be better at higher deposition rates. As seen in figure 14, the resistivity decreases with increasing deposition rate. One interpretation of this result is that the Mo films are denser at the higher rates. However, this poses a dilemma. If the films are denser, they

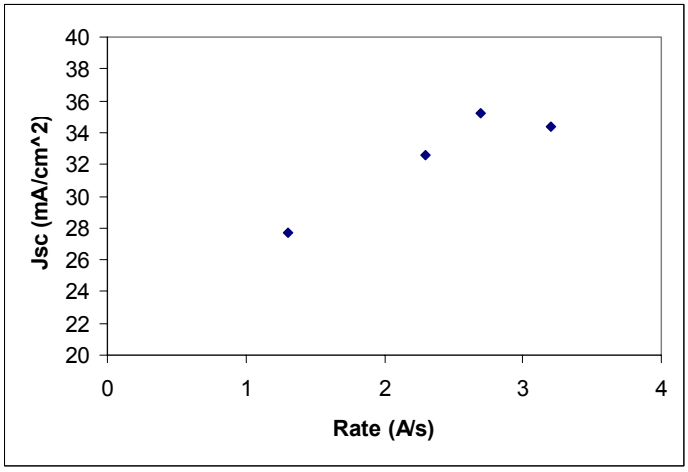

Figure 13. Dependence of Jsc on Mo deposition rate for CIGS devices.

should allow less Na through, and in reference to the discussion of figure 11 above, this should result in lower Jsc's at higher deposition rates. Taken together these results suggest that stress is also playing a role in interpreting the data of figure 11 for Jsc as it does for Voc vis a vis figure 12. Thus we might speculate that both thinner Mo and Mo deposited at higher rates results in increased stress, and this enhances Jsc. The correlations we have seen with measured Na content so far also suggest a role for Na. Further effort will be required to sort this out and understand what each is contributing.

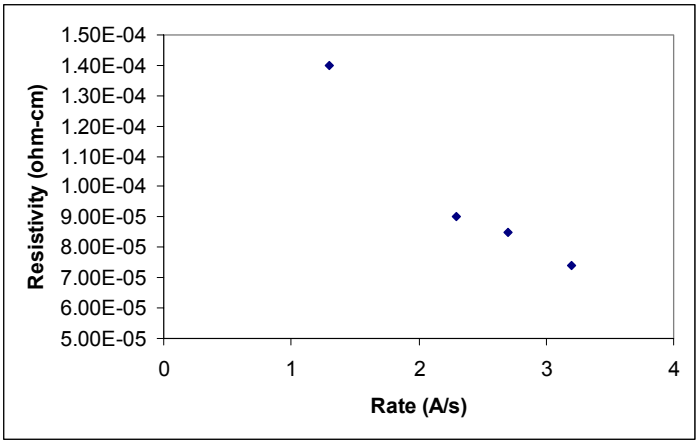

Figure 14. Dependency of Mo resistivity on deposition rate.

In figure 15 we show the effect of deposition rate on spectral response for the devices from figure 13 deposited at low(1.3 Å/s) and high(3.2 Å/s) deposition rates. As can be seen, there is an overall upward shift in the QE spectrum at high rates. We have simulated such behavior in the past and have found it to be explainable in terms of interface defects. This might be attributed to Na catalyzed defect formation in the interface region. It is not clear how to understand the role of stress in this regard.

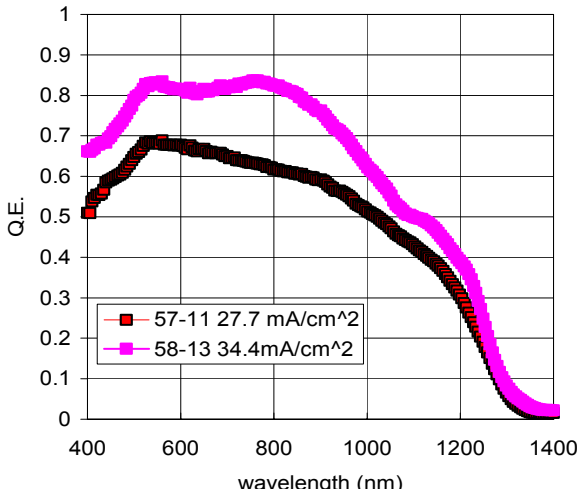

Figure 15. QE response for CIGS devices deposited at high(58-13) and low(57-11) Mo

Yet another contributing operational parameter for Mo deposition is the target voltage. As a new target breaks in the voltage required to maintain a desired deposition rate is constantly changing. Our typical standard deposition rate is about 2 Å/s. To reach this level with a new target results in target voltages in excess of 600 volts. The effect this has on Voc is shown in figure 16. The deposition rate for this range of discharge voltages is 2 – 3 Å/s which is good for Jsc as per figure 13, however, this range is clearly not acceptable for Voc. The data points between 600 and 700 volts are from a new target that is not yet broken in. The data point at 400 volts is for a target that has been broken in. The lower discharge voltage results in higher Voc. In this case the deposition rate is in the same 2 – 3 Å/s range, so Jsc's will also be high. At a practical level this indicates that it is important to break a new Mo target in before depositing films. However, this can take a lot of time and waste a lot of Mo, so it is important to understand the underlying mechanisms so that run conditions can be adjusted with a new target to cut down on this waste of time and material.

In consideration of previous efforts to modify the back contact the strong dependence on Voc on the sputtering target voltage is surprising. In our simulations we showed that the back contact energy can have an effect on Voc. We tried numerous experiments to alter the back contact energy and were successful only in sending it in the wrong direction. The above results, however, may be thought of in these terms. A high target discharge voltage during Mo

deposition results in an unfavorable back contact energy. More effort will be required to determine the nature of the Voc dependence and to understand the film growth mechanisms that cause it.

One additional piece of data that is useful in sorting out the role of Na is provided in figure 17. This is the Voc and FF profile for the 5 x 5 array of devices that we deposit on the 2" x 2" substrate. During CIGS deposition the Cu source is at the top, In at the bottom, Ga to the left, and Se to the right. For our purposes here we note that the devices at the top have more Cu than those at the bottom. For this sample the Mo thickness was 6000 Á, evenly split between high and low pressure deposition. This reduced Mo thickness is expected to let more Na through to the CIGS layers. The Na catalyzed In oxidation mechanism is reported to be more active in a Cu-deficient region[13], and the possible replacement of Cu by Na would also be expected to be more active in a Cu-deficient region as well. Thus we might expect to see a top to bottom dependence in the above array. The absence of such a dependence suggests that Na might not be the dominant parameter under these conditions. To first order stress would not seem to be dependent on the metal ratios in the CIGS, so its influence would not be expected to result in gradients. At this point it seems that stress has the upper hand in terms of understanding the Mo deposition data. These are important findings in that the defect structure is strongly influenced by the growth surface and therefore not necessarily limited by inherent properties due to the two-step growth process. In the next phase of this project we hope to discover means of improving performance through better control of substrate properties.

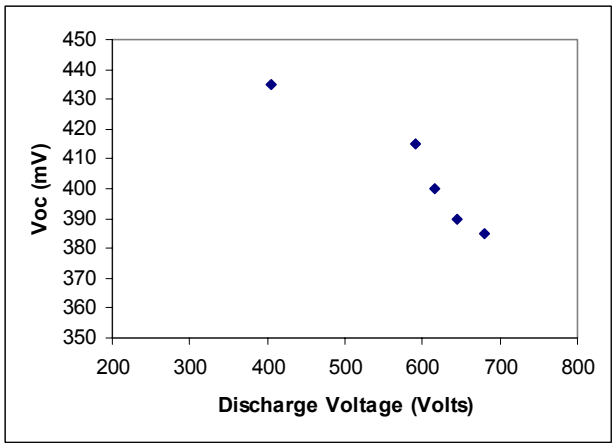

Figure 16. Dependence of Voc on sputtering target discharge voltage for CIGS devices.

420 57%	450 62%	440 59%	430 57%	390 50%
450 54%	460 61%	450 55%	450 58%	430 53%
450 51%	430 52%	420 52%	440 53%	420 49%
450 54%	440 54%	390 53%	400 52%	420 45%
410 48%	440 56%	420 49%	430 56%	270 35%

Figure 17. Voc and FF profile for CIGS on 6000 A Mo. The Cu source during CIGS deposition is at

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© - AMPS is a first principles simulation code developed by Penn State/EPRI.

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